PRELIMINARY | Data Sheet | February 2000 | File Number 4557.2

Four-Channel Programmable Digital DownConverter

The HSP50216 Quad Programmable Digital DownConverter (QPDC) is designed for high dynamic range applications such as cellular basestations where multiple channel processing is required in a small physical space. The QPDC combines into a single package, a set of four channels which include: digital mixers, a quadrature carrier NCO, digital filters, a resampling filter, a Cartesian-to-polar coordinate converter and an AGC loop.

The HSP50216 accepts four channels of 16-bit real digitized IF samples which are mixed with local quadrature sinusoids. Each channel carrier NCO frequency is set independently by the microprocessor. The output of the mixers are filtered with a CIC and FIR filters, with a variety of decimation options. Gain adjustment is provided on the filtered signal. The digital AGC provides a gain adjust range of up to 96dB with programmable thresholds and slew rates. A cartesian to polar coordinate converter provides magnitude and phase outputs. A frequency discriminator provides a frequency output via the FIR filter. Selectable outputs include I samples, Q samples, Magnitude, Phase, Frequency and AGC gain. The output resolution is selectable from 4-bit fixed point to 32-bit floating point.

The maximum output bandwidth achievable using a single channel is at least 1MHz.

Features

- Up to 70MSPS Input
- Four Independently Programmable Downconverter Channels in a single package
- Four Parallel 16-Bit Inputs -Fixed or Floating Point Format
- 32-Bit Programmable Carrier NCO with > 115dB SFDR
- 110dB FIR Out of Band Attenuation
- Decimation from 8 to >65536
- 24-bit Internal Data Path
- Digital AGC with up to 96dB of Gain Range
- Filter Functions
  - 1 to 5 Stage CIC Filter
  - Halfband Decimation and Interpolation FIR Filter
  - Programmable FIR Filter
  - Resampling FIR Filter
- Cascadable Filtering for Additional Bandwidth
- Four Independent Serial Outputs
- 3.3V Operation

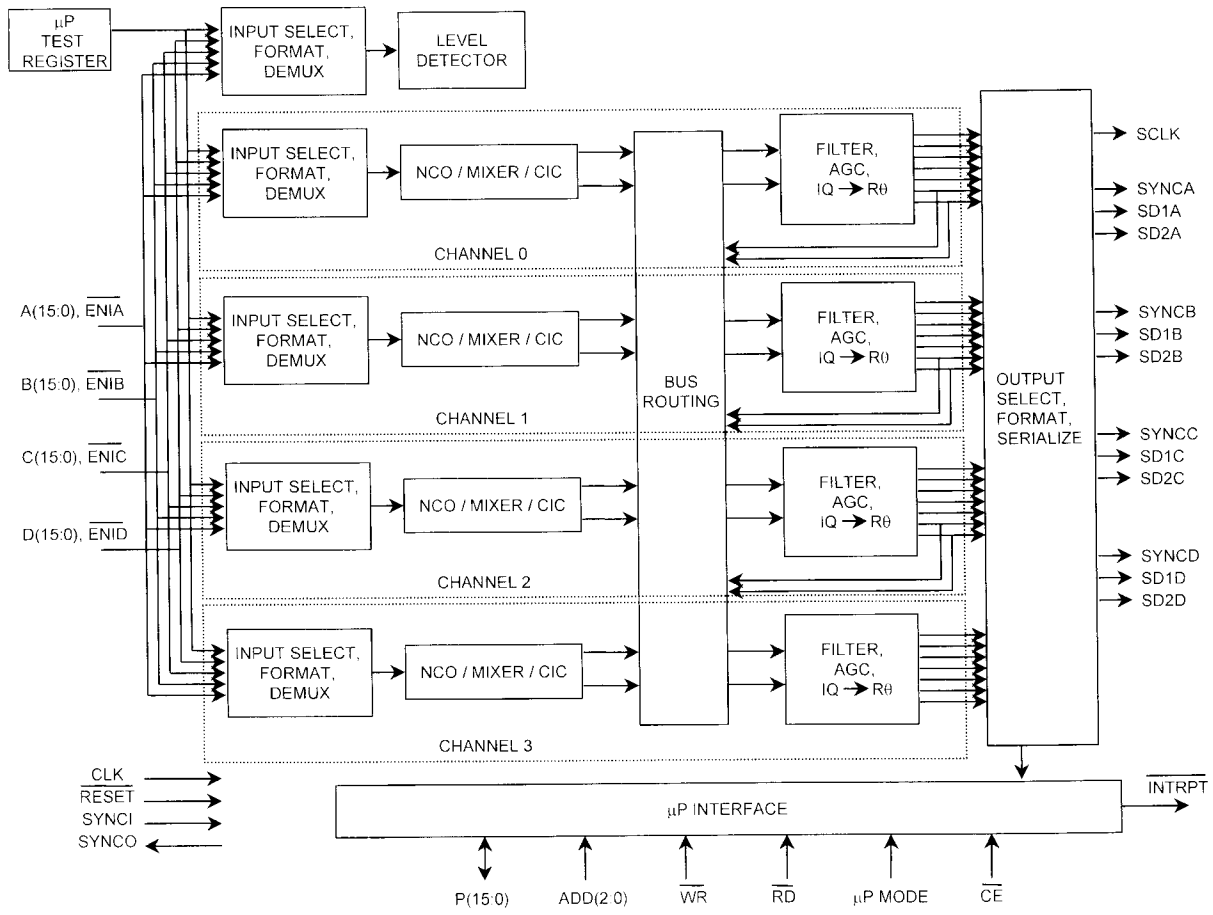
Applications

- Narrow-Band TDMA through IS-95 CDMA Digital Software Radio and Basestation Receivers

Ordering Information

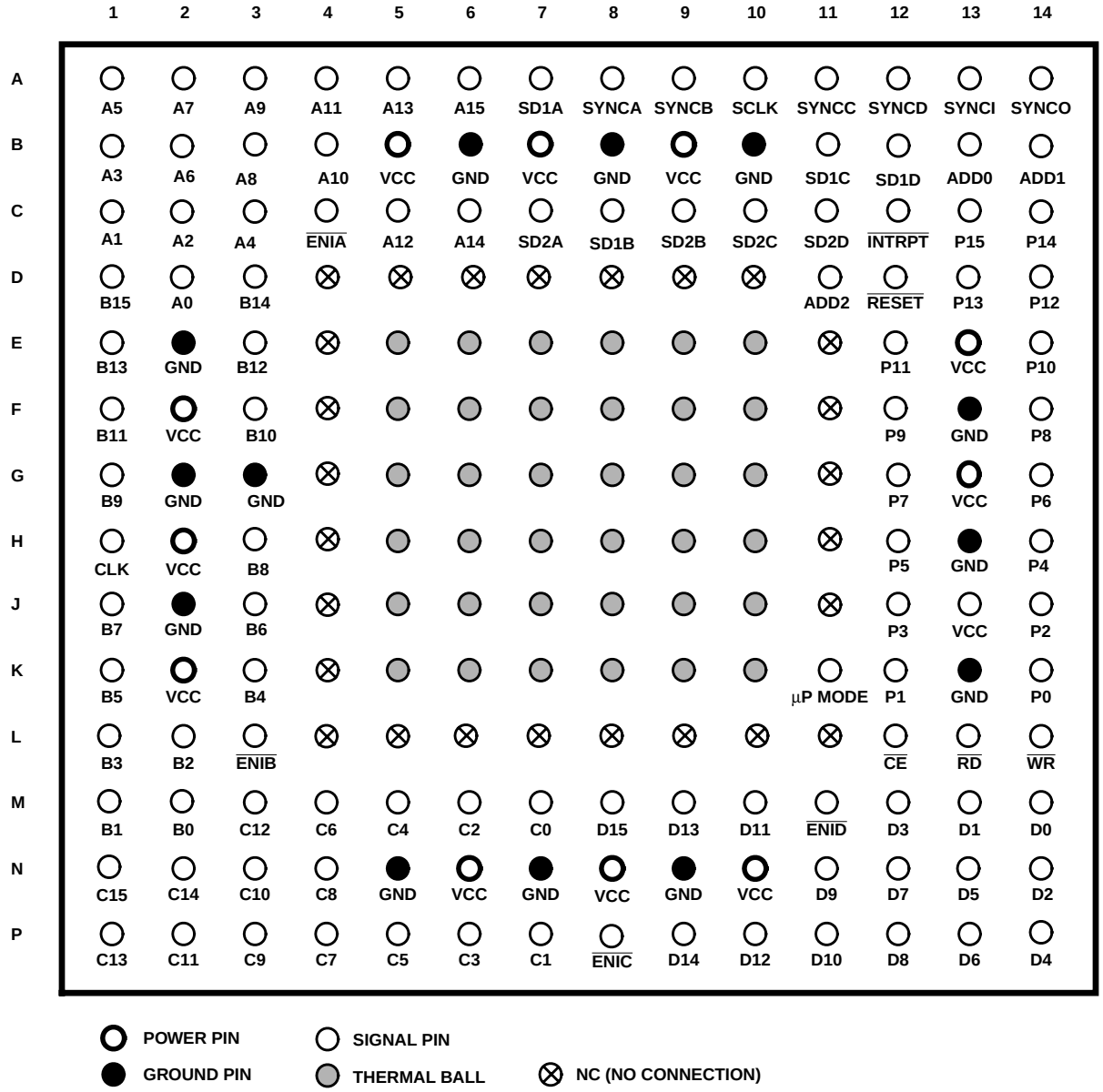
PART NUMBER	TEMP RANGE (^{o}C)	PACKAGE	PKG. NO
HSP50216KI	-40 to +85	196 Ld BGA	V196.12x12

Block Diagram



Pinout

196 LEAD BGA
TOP VIEW



Pin Descriptions

NAME	TYPE	DESCRIPTION
POWER SUPPLY		
VCC	-	Positive Power Supply Voltage, 3.3V ±0.15
GND	-	Ground, 0V.
INPUTS		
A(15:0)	I	Parallel Data Input bus A. Sampled on the rising edge of clock when $\overline{\text{ENIA}}$ is active (low).
B(15:0)	I	Parallel Data Input bus B. Sampled on the rising edge of clock when $\overline{\text{ENIB}}$ is active (low).
C(15:0)	I	Parallel Data Input bus C. Sampled on the rising edge of clock when $\overline{\text{ENIC}}$ is active (low).
D(15:0)	I	Parallel Data Input bus D. Sampled on the rising edge of clock when $\overline{\text{ENID}}$ is active (low).
$\overline{\text{ENIA}}$	I	Input enable for Parallel Data Input bus A. Active low. This pin enables the input to the part in one of two modes, gated or interpolated. In gated mode, one sample is taken per CLK when $\overline{\text{ENI}}$ is asserted.
$\overline{\text{ENIB}}$	I	Input enable for Parallel Data Input bus B. Active low. This pin enables the input to the part in one of two modes, gated or interpolated. In gated mode, one sample is taken per CLK when $\overline{\text{ENI}}$ is asserted.
$\overline{\text{ENIC}}$	I	Input enable for Parallel Data Input bus C. Active low. This pin enables the input to the part in one of two modes, gated or interpolated. In gated mode, one sample is taken per CLK when $\overline{\text{ENI}}$ is asserted.
$\overline{\text{ENID}}$	I	Input enable for Parallel Data Input bus D. Active low. This pin enables the input to the part in one of two modes, gated or interpolated. In gated mode, one sample is taken per CLK when $\overline{\text{ENI}}$ is asserted.
CONTROL		
CLK	I	Input clock. All processing in the HSP50216 occurs on the rising edge of CLK.
SYNCI	I	Synchronization Input Signal. Used to align the processing with an external event or with other HSP50216 devices. SYNCI can update the carrier NCO, reset decimation counters, restart the filter compute engine, and restart the output section among other functions. For most of the functional blocks, the response to SYNCI is programmable and can be enabled or disabled.
SYNCO	O	Synchronization Output Signal. The processing of multiple HSP50216 devices can be synchronized by tying the SYNCO from one HSP50216 device (the master) to the SYNCI of all the HSP50216 devices (the master and slaves).
$\overline{\text{RESET}}$	I	Reset Signal. Active low. Asserting reset will halt all processing and set certain registers to default values.
OUTPUTS		
SD1A	O	Serial Data Output 1A. A serial data stream output which can be programmed to consist of I1, Q1, I2, Q2, magnitude, phase, frequency ($d\phi/dt$), AGC gain, and/or zeros. In addition, data outputs from Channels 0, 1, 2 and 3 can be multiplexed into a common serial output data stream. Information can be sequenced in a programmable order. *See Serial Data Output Formatter Section and Microprocessor Interface Section.*
SD2A	O	Serial Data Output 2A. This output is provided as an auxiliary output for Serial Data Output 1A to route data to a second destination or to output two words at a time for higher sample rates. SD2A has the same programmability as SD1A except that floating point format is not available. *See Serial Data Output Formatter Section and Microprocessor Interface Section.*
SD1B	O	Serial Data Output 1B. See description for SD1A.
SD2B	O	Serial Data Output 2B. See description for SD2A.
SD1C	O	Serial Data Output 1C. See description for SD1A.
SD2C	O	Serial Data Output 2C. See description for SD2A.
SD1D	O	Serial Data Output 1D. See description for SD1A.
SD2D	O	Serial Data Output 2D. See description for SD2A.
SCLK	O	Serial Output Clock. Can be programmed to be at 1, 1/2, 1/4, 1/8, or 1/16 times the clock frequency. The polarity of SCLK is programmable.
SYNCA	O	Serial Data Output 1A sync signal. This signal is used to indicate the start of a data word and/or frame of data. The polarity and position of SYNCA is programmable.

Pin Descriptions (Continued)

NAME	TYPE	DESCRIPTION
SYNCB	O	Serial Data Output 1B sync signal. This signal is used to indicate the start of a data word and/or frame of data. The polarity and position of SYNCB is programmable.
SYNCC	O	Serial Data Output 1C sync signal. This signal is used to indicate the start of a data word and/or frame of data. The polarity and position of SYNCC is programmable.
SYNCD	O	Serial Data Output 1D sync signal. This signal is used to indicate the start of a data word and/or frame of data. The polarity and position of SYNCD is programmable.
MICROPROCESSOR INTERFACE		
P(15:0)	I/O	Microprocessor Interface Data bus. *See Microprocessor Interface Section*. P15 is the MSB.
ADD(2:0)	I	Microprocessor Interface Address bus. ADD2 is the MSB. *See Microprocessor Interface Section*. Note: ADD2 **is not** used but designated for future expansion.
$\overline{WR}$	I	Microprocessor Interface Write Signal. The data on P(15:0) is written to the destination selected by ADD(2:0) on the rising edge of $\overline{WR}$ when $\overline{CE}$ is asserted (low). *See Microprocessor Interface Section*.
$\overline{RD}$	I	Microprocessor Interface Read Strobe. The data at the address selected by ADD(2:0) is placed on P(15:0) when $\overline{RD}$ is asserted (low) and $\overline{CE}$ is asserted (low). *See Microprocessor Interface Section*.
µP MODE	I	Microprocessor Interface Mode Control. This pin is used to select the Read/Write mode for the Microprocessor Interface.
$\overline{CE}$	I	Microprocessor Interface Chip Select. Active low. This pin has the same timing as the address pins.
$\overline{INTRPT}$	O	Microprocessor Interrupt Signal. Asserted for a programmable number of clock cycles when new data is available on the selected Channel.

Functional Description

The HSP50216 is a four channel digital receiver integrated circuit offering exceptional dynamic range and flexibility. Each of the four channels consists of a front-end NCO/digital mixer/CIC-filter block and a back-end FIR/AGC/polar-conversion block. The parameters for the four channels are independently programmable. Four parallel data input busses (A(15:0), B(15:0), C(15:0) and D(15:0)) and four serial data outputs (SDxA, SDxB, SDxC, and SDxD; x = 1 or 2) are provided. Each input can be connected to any or all of the internal signal processing channels, Channels 0, 1, 2 and 3. The output of each channel can be routed to any of the serial outputs. Outputs from more than one channel can be multiplexed through a common output if the channels are synchronized. The four channels share a common input clock and a common serial output clock, but the output sample rates can be synchronous or asynchronous. Bus multiplexers between the front end and back end sections provide flexible routing between channels for cascading back-end filters or for routing one front end to multiple back ends for polyphase filtering (to provide wider bandwidth filtering). A level detector is provided to monitor the signal level on any of the parallel data input busses.

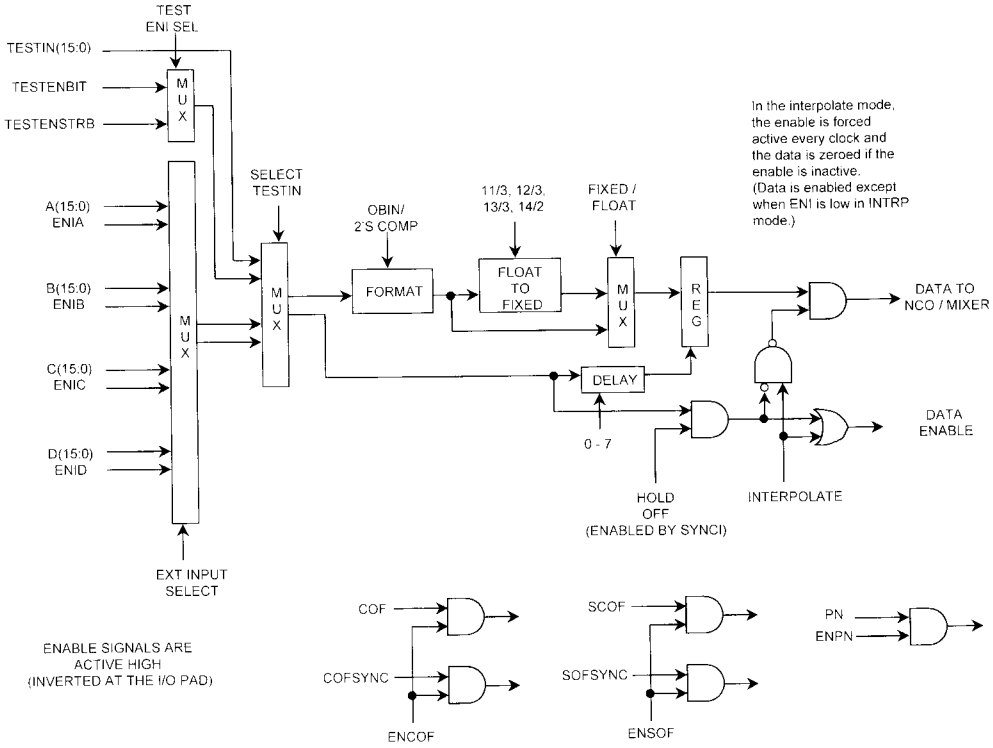
Each front end NCO/digital mixer/CIC filter section includes a quadrature numerically controlled oscillator (NCO), digital mixer, and a cascaded-integrator-comb filter (CIC). The NCO has a 32-bit frequency control word for 16.3MHz tuning resolution at an input sample rate of 70MSPS. The SFDR of the NCO is >115dB. The CIC filter order is programmable between 1 and 5 and the CIC decimation factor can be programmed from 4 to 65536, depending on the number of stages selected.

Each back end section includes an FIR processing block, an AGC and a cartesian-to-polar coordinate converter. The FIR processing block is a flexible filter compute engine that can compute a single FIR or a set of filters. A single filter in a chain can have up to 256 taps and the total number of taps in a set of filters can be up to 384. The filter compute engine supports a variety of filter types including decimation, interpolation and resampling filters. The coefficients for the programmable digital filters are 22 bits wide. Coefficients are provided in ROM for several halfband filter responses and for a resampler. The AGC section can provide up to 96dB of either fixed or automatic gain control. For automatic gain control, two settling modes and two sets of loop gains are provided. Separate attack and decay slew rates are provided for each loop gain. Programmable limits allow the user to select a gain range less than 96dB. The outputs of the cartesian-to-polar coordinate conversion block, used by the AGC loop, are also provided as outputs to the user for demodulation.

The HSP50216 supports both fixed and floating point parallel data input modes. The floating point modes support gain ranging A/D converters. Gated, interpolated and multiplexed data input modes are supported. The serial data output word width for each data type can be programmed to one of ten output bit widths from 4-bit fixed point through 32-bit IEEE floating point.

The HSP50216 is programmed through a 16-bit microprocessor interface. The output data can also be read via the microprocessor interface for all channels that are synchronized. The HSP50216 is specified to operate to a maximum clock rate of 70MSPS over the industrial temperature range (-40^{o}C to 85^{o}C). The power supply voltage range is 3.3V ± 0.15V. The I/Os **are not** 5V tolerant.

Input Select/Format Block



Each front end block and the level detector block contains an input select/format block. A functional block diagram is provided in the above figure. The input source can be any of the four parallel input busses (see Microprocessor Interface Section Table 1, IWA *000h) or a test register loaded via the processor bus (see Microprocessor Interface Section Table 40, GWA F807h).

The input to the part can operate in a gated or interpolated mode. Each input channel has an input enable ($\overline{ENIx}$, x = A, B, C or D). In the gated mode, one input sample is processed per clock that the $\overline{ENIx}$ signal is asserted (low). Processing is disabled when $\overline{ENIx}$ is high. The $\overline{ENIx}$ signal is pipelined through the part to minimize delay (latency). In the interpolated mode, the input is zeroed when the $\overline{ENIx}$ signal is high, but processing inside the part continues. This mode inserts zeros between the data samples, interpolating the input data stream up to the clock rate. On reset, the part is set to gated mode and the input enables are disabled. The inputs are enabled by the first SYNCI signal.

The input section can select one channel from a multiplexed data stream of up to 8 channels. The input enable is delayed by 0 to 7 clock cycles to enable a selection register. The register following the selection register is enabled by the non-delayed input enable to realign the processing of the channels. The one-clock-wide input enable must align with the data for the first channel. The desired channel is then selected by programming the delay. A delay of zero selects the first channel, a delay of 1 selects the second, etc.

The parallel input busses are 16 bits wide. The input format may be twos complement or offset binary format. A floating point mode is also supported. The floating point modes and the mapping of the parallel 16-bit input format is discussed below.

Floating Point Input Mode Bit Mapping

The input bit weighting for fixed point is 2^{0} (corresponding to parallel input bus A, B, C or D bit 15) to 2^{-15} (corresponding to parallel input bus A, B, C or D bit 0). For floating point modes, the least significant 2 or 3 bits are used as exponent bits (See Floating Point Input Mode Bit Mapping Tables). The difference between the four floating point modes with three exponent bits is where the exponent saturates.

Floating Point Input Mode Bit Mapping Tables

A, B, C or D(15:0) Input: 2^ - 0 1 2 3 4 5 6 7 8 9 10 11 12 13(exp2) 14(exp1) 15(exp0)

11-BIT MODE: 11-BIT MANTISSA (MINIMUM), 3-BIT EXPONENT, 30dB EXPONENT RANGE

EXPONENT	GAIN (dB)	PIN BIT WEIGHTING TO 16-BIT INPUT MAPPING, 2^-
000	0	0 0 0 0 0 0 1 2 3 4 5 6 7 8 9 10
001	6	0 0 0 0 0 1 2 3 4 5 6 7 8 9 10 11
010	12	0 0 0 0 1 2 3 4 5 6 7 8 9 10 11 12
011	18	0 0 0 1 2 3 4 5 6 7 8 9 10 11 12 z
100	24	0 0 1 2 3 4 5 6 7 8 9 10 11 12 z z
101 (Note 1)	30	0 1 2 3 4 5 6 7 8 9 10 11 12 z z z

NOTE:

1. Or 110 or 111, the exponent input saturates at 101.

12-BIT MODE: 12-BIT MANTISSA, 3-BIT EXPONENT, 24dB EXPONENT RANGE

EXPONENT	GAIN (dB)	PIN BIT WEIGHTING TO 16-BIT INPUT MAPPING, 2^-
000	0	0 0 0 0 0 1 2 3 4 5 6 7 8 9 10 11
001	6	0 0 0 0 1 2 3 4 5 6 7 8 9 10 11 12
010	12	0 0 0 1 2 3 4 5 6 7 8 9 10 11 12 z
011	18	0 0 1 2 3 4 5 6 7 8 9 10 11 12 z z
100 (Note 2)	24	0 1 2 3 4 5 6 7 8 9 10 11 12 z z z

NOTE:

2. Or 101, 110, or 111, the exponent input saturates at 100.

13-BIT MODE: 13-BIT MANTISSA, 3-BIT EXPONENT, 18dB EXPONENT RANGE

EXPONENT	GAIN (dB)	PIN BIT WEIGHTING TO 16-BIT INPUT MAPPING, 2^-
000	0	0 0 0 0 1 2 3 4 5 6 7 8 9 10 11 12
001	6	0 0 0 1 2 3 4 5 6 7 8 9 10 11 12 z
010	12	0 0 1 2 3 4 5 6 7 8 9 10 11 12 z z
011 (Note 3)	18	0 1 2 3 4 5 6 7 8 9 10 11 12 z z z

NOTE:

3. Or 100, 101, 110, or 111, the exponent input saturates at 011.

14-BIT MODE: 14-BIT MANTISSA, 2-BIT EXPONENT, 12dB EXPONENT RANGE

EXPONENT	GAIN (dB)	PIN BIT WEIGHTING TO 16-BIT INPUT MAPPING, 2^-
00	0	0 0 0 1 2 3 4 5 6 7 8 9 10 11 12 13
01	6	0 0 1 2 3 4 5 6 7 8 9 10 11 12 13 z
10 (Note 4)	12	0 1 2 3 4 5 6 7 8 9 10 11 12 13 z z

NOTE:

4. Or 11, the exponent input saturates at 10.

Level Detector

An input level detector is provided to monitor the signal level on any of the input busses. Which input bus, the input format, and the level detection type are programmable (see Microprocessor Interface Section Tables 37, 38 and 39, GWA's F804h, F805h and F806h). The supported monitoring modes are: integrated magnitude (like the HSP50214 w/o the threshold), leaky integration ($Y_n = X_n \times A + Y_{n-1} \times (1-A)$), and peak detection. The measurement interval can be programmed from 2 to 65537 samples (or continuous for the leaky integrator and peak detect cases). The output is 32 bits and is read via the µP interface.

NCO/Mixer

After the input select/format section, the samples are multiplied by quadrature sine wave samples from the carrier NCO. The NCO has a 32-bit frequency control, providing sub-hertz resolution at the maximum clock rate. The quadrature sinusoids have exceptional purity. The purity of the NCO should not be the determining factor for the receiver dynamic range performance. The phase quantization to the sine/cosine generator is 24 bits and the amplitude quantization is 19 bits.

The carrier NCO center frequency is loaded via the µP bus. The center frequency control is double buffered - the input is loaded into a center frequency holding register via the µP interface. The data is then transferred from the holding register to the active register by a write to a address IWA *006h or by a SYNCI signal, if loading via SYNCI is enabled. To synchronize multiple channels, the carrier NCO phase accumulator feedback can be zeroed on loading to restart all of the NCOs at the same phase. A serial offset frequency input is also available for each channel through the D(15:0) parallel data input bus (if that bus is not needed for data input). This is legacy support for HSP50210 type tracking signals.

After the mixers, a PN signal can be added to the data. This feature is provided for test and to digitally reduce the input sensitivity and adjust the receiver range (sensitivity). The effect is the same as increasing the noise figure of the receiver, reducing its sensitivity and overall dynamic range. The one bit PN data is scaled by a 16-bit programmable scale factor. The overall range for the PN is 0 to 1/8 full scale. A gain of 0 disables the PN input. The bit weighting for the gain is:

SIGNAL (2^-):

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20

PN (2^):

S S S X X X X X X X X X X X X X X X X

GAIN REG (2^):

X X X X X X X X X X X X X X X X

(A POSITIVE 16-BIT VALUE IS LOADED, S = SIGN)

The minimum, non-zero, PN value is $1/(2^{18})$ of full scale (-108dBFS) on each axis (-105dBFS total). For an input noise level of -75dBFS, this allows the SNR to be decreased in steps of 1/8dB or less. The I and Q PN codes are offset in time to decorrelate them. The PN code is selected and enabled in the test control register (F800h). The PN is added to the signal after the mix as:

Bit Weights	0.	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	6	7	8	9
Input Bits	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X
PN Value ±	0	0	0	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P	P

so the maximum level is -12dBFS and the minimum, non-zero level is -108dBFS. The PN code can be 2^{15}-1, 2^{23}-1 or 2^{15}-1 * 2^{23}-1.

CIC Filter

Next, the signal is filtered by a cascaded integrator/comb (CIC) filter. A CIC filter is an efficient architecture for decimation filtering. The power or magnitude squared frequency response of the CIC filter is given by:

$$P(f) = \left(\frac{\sin(\pi M f)}{\sin\left(\frac{\pi f}{R}\right)} \right)^{2N}$$

where

M = Number of delays (1 for the HSP50216)

N = Number of stages

and R = Decimation factor.

The CIC filter order is programmable from 0 to 5. The minimum decimation is 4. If the order is set to 0, there must be at least 4 clocks between samples or the decimation counter must be set to 4 to chose every 4th sample. The integrator/comb bit widths are:

69, 62, 53, 44, 34, 32, 32, 32, 32, 32.

The integrators are sized for decimation factors up to 512 with 5 stages. The maximum decimation varies with the number of stages, but the maximum is 65536, limited by the decimation counter.

A CIC filter has a gain of R^N, where R is the decimation factor and N is the number of stages. For a 5 stage CIC, the gain is R^5. The number of input bits is 24. The decimation factors that a CIC can handle depends on the sizes of the integrators. The integrators are sized to prevent more than one rollover per decimation period. In the HSP50216, the integrators are slightly oversized to reduce the quantization noise at each stage.

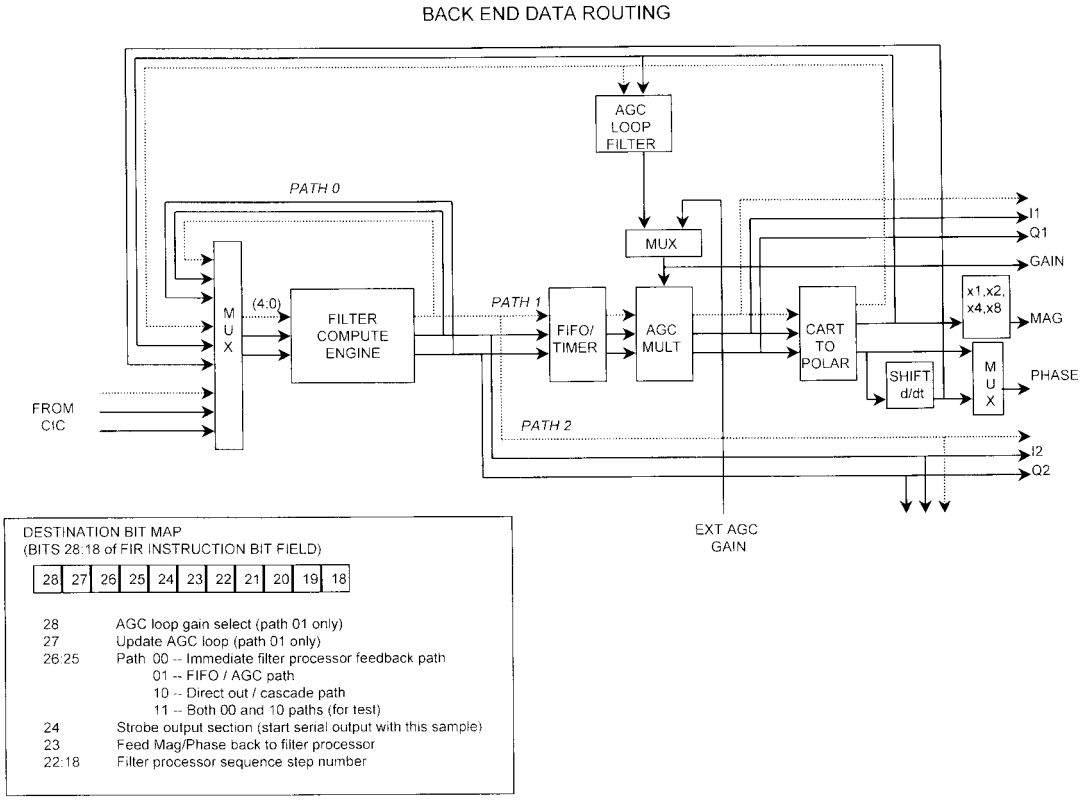
Because the CIC filter gain can vary greatly with decimation, a barrel shifter is provided ahead of the CIC to add gain to the input signal. The shift factor is adjusted to keep the total barrel shifter and CIC filter between 0.5 and 1.0. The shift

factor can be from 0 to 31. The equation used to compute the shift factor is:

Shift Factor = 45 - Ceiling($\log_2(R^N)$).

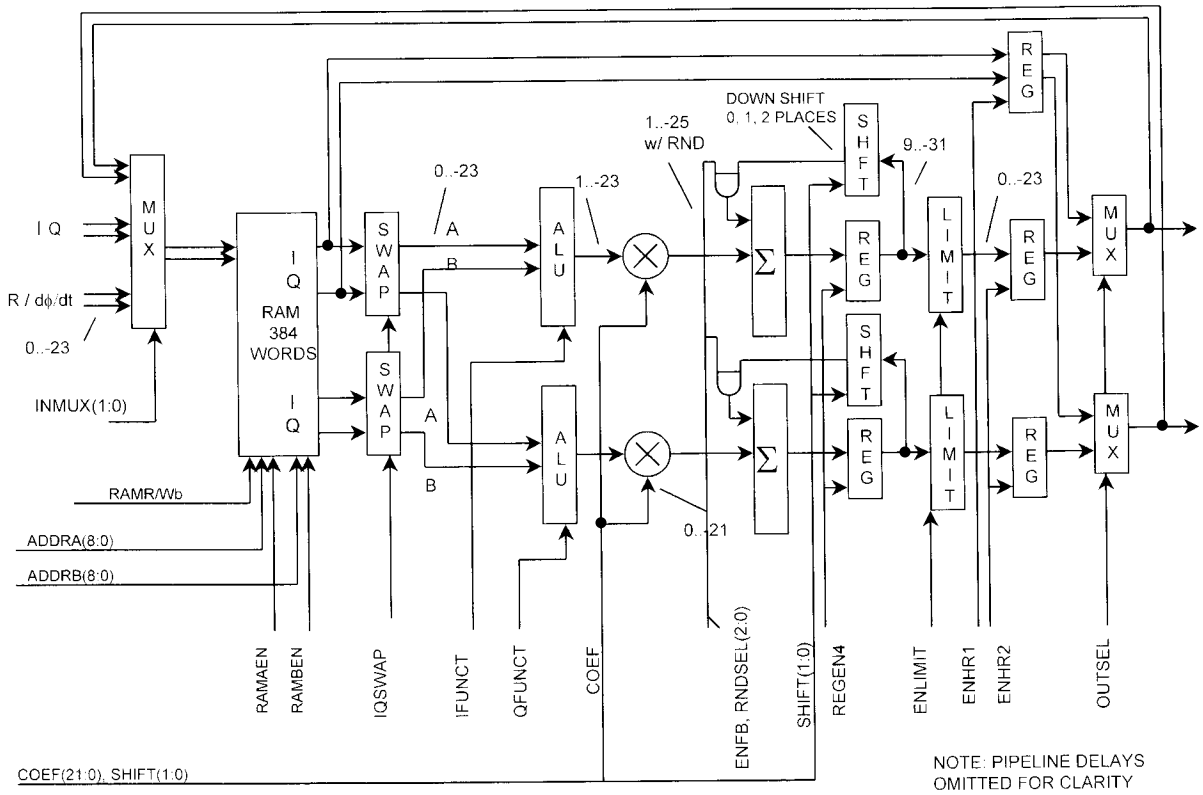
NOTE: With a CIC order of zero, the CIC shifter does not have sufficient range to route more than 10 bits to the back end.

Back End Section



One back-end processing section is provided per channel. Each back end section consists of a filter compute engine, a FIFO for rate smoothing, an AGC and a cartesian-to-polar coordinate conversion block. A block diagram showing the major functional blocks and data routing is shown above. The data input to the back end section is through the filter compute engine. There are two other inputs to the filter compute engine, they are a data recirculation path for cascading filters and a magnitude and dϕ/dt feedback path for AM and FM filtering. There are seven outputs from each back end processing section. These are I and Q directly out of the filter compute engine (I2, Q2), I and Q passed through the FIFO and AGC multipliers (I1, Q1), magnitude (MAG), phase (or dϕ/dt), and the AGC gain control value (GAIN). The I2/Q2 outputs are used when cascading back end stages. The routing of signals within the back end processing section is controlled by the filter compute engine. The routing information is embedded in the instruction bit fields used to define the digital filter being implemented in the filter compute engine.

Filter Compute Engine



The filter compute engine is a dual multiply-accumulator (MAC) data path with a microcoded FIR sequencer. The filter compute engine can implement a single FIR or a set of filters. For example, the filter chain could include two halfband filters, a shaping (matched) filter and a resampling filter. The following filter types are currently supported by the architecture and microcode:

- even symmetric w/ even # of taps decimation filters
- even symmetric w/ odd # of taps decimation filters (including HBFs)
- odd symmetric w/ even # of taps decimation filters
- odd symmetric w/ odd # of taps decimation filters
- asymmetric decimation filters
- complex filters
- interpolation filters (up to interpolate by 4)
- interpolation halfband filters
- resampling filters (under NCO control)
- fixed resampling ratio filter (within the available number of coefficients)
- quadrature to real filtering (w/ fs/4 up conversion)

The input to the filter compute engine comes from one of three sources - a CIC filter output (which can also be another backend section), the output of the filter compute engine (fed back to the input) or the magnitude and dϕ/dt fed back from the cartesian-to-polar coordinate converter.

The number and size of the filters in the chain is limited by the number of clock cycles available and by the data and coefficient RAM/ROM resources. The data RAM is 384 words (I/Q pairs) deep. The data addressing is modulo in power-of-2 blocks, so the maximum filter size is 256. The block size and the block starting memory address for each filter is programmable so that the available memory can be used efficiently. The coefficient RAM is 192 words deep. It is half the size of the data memory because filter coefficients are typically symmetric. ROMs are provided with halfband filter coefficients, resampling filter coefficients, and constants. The filter compute engine exploits symmetry where possible so that each MAC can compute two filter taps per clock, by doing a pre-add before multiplying. In the case of halfband filters, the zero-valued coefficients are skipped for extra efficiency. There is an overhead of one clock cycle per input sample for each filter in the chain (for writing the data into the data RAM) and (except in special cases) a two clock cycle overhead for the entire chain for program flow control instructions.

The output of the filter compute engine is routed through a FIFO in the main output path. The FIFO is provided to more evenly space the FIR outputs when they are produced in

bursts (as when computing interpolation filters). The FIFO is four samples deep. The FIFO is loaded by the output of the filter when that path is selected. It is unloaded by a counter. The spacing of the output samples is specified in clock periods. The spacing can be from 1 (fall through) to 4096 samples (approximately the spacing for a 16KSPS output sample rate when using 65MSPS clock).

The number and order of the filtering in the filter chain is defined by a FIR control program. The FIR control program is a sequence of up to 32 instruction words. Each instruction word can be a filter or program flow instruction. The filter instruction defines a FIR in the chain, specifying the type of FIR, number of taps, decimation, memory allocation, etc. For program flow, a wait for input sample(s) instruction, a loop counter load, and several jumps (conditional and unconditional) are provided.

The simplest filter program computes a single filter. It has three instructions (see Sample Filter #1Program Instructions below):

SAMPLE FILTER #1 PROGRAM

STEP	INSTRUCTION
0	Wait for enough input samples (equal to the decimation factor)
1	FIR Type = even symmetric 95 taps Dec x 2 Compute one output Decrement wait counter Memory block size 128 Memory block start at 64, Coefficient block start at 64 Step size 1 Output to AGC
2	Jump, Unconditional, to step 0

The parameters of the FIR (including type, number of taps, decimation and memory usage) are specified in the bit fields of the step 2 instruction word. To change the filtering the only other change needed is the number of samples in the wait threshold register. The filter in this example requires 52 clock cycles to compute, allocated as follows:

SAMPLE FILTER #1 CLOCK CYCLES CALCULATION

CLOCK CYCLES	FUNCTION PERFORMED
48	Clocks for FIR computation (two taps/clock due to symmetry)
2	Clocks for writing the input data into the data RAMs (Decimate by 2 requires 2 inputs per output)
2	Clocks for the program flow instructions (wait and jump)
52	Total

Using a 65MSPS clock, the output sample rate could be as high as 1.25MSPS. The input sample rate from the CIC filter would be 2.5MSPS. The impulse response length would be 38 μsec (95 taps at 0.4μs/tap).

Each additional filter added to the signal processing chain requires one instruction step. As an example of this, a typical filter chain might consist of two decimate-by-2 halfband filters being followed by a shaping filter with the final filter being a resampling filter. The program for this case might be (see Sample Filter Program #2 Instructions below):

SAMPLE FILTER #2 PROGRAM

STEP	INSTRUCTION
0	Wait for enough input samples (usually equal to the total decimation - 8 in this case)
1	FIR Type = even symmetry 15 taps Halfband Dec x 2 Compute four outputs Memory block size 32 Memory block start at 0 Coefficient block start at 13 Output to step 2 Decrement wait count
2	FIR Type = even symmetry 23 taps Halfband Dec x 2 Compute two outputs Memory block size 32 Memory block start at 32 Coefficient block start at 24 Output to step 3
3	FIR Type = even symmetry 95 taps Dec x 2 Compute one output Memory block size 128 Memory block start at 64 Coefficient block start at 64 Step size 1 Output to step 4
4	FIR Type = resampler Increment NCO 6 taps Compute one output Memory block size 8 Memory block starts at 192 Coefficient block start at 512 Step size 32 Output to AGC
5	Jump, Unconditional, to 0

Sample filter #2 requires:

- 32 + 32 + 128 + 8 = 200 data RAM locations
- (95+1)/2=48 coefficient RAM location (resampler and HBF coefficient are in ROM).

The number of clock cycles required to compute an output for Sample filter #2 is calculated as follows:

SAMPLE FILTER #2 CLOCK CYCLES CALCULATION

CLOCK CYCLES	FUNCTION PERFORMED
20	Halfband 1 compute clocks (5 per compute x4 computes)
8	Halfband 1 input sample writes
14	Halfband 2 compute clocks (7 per compute x2 computes)
4	Halfband 2 input sample writes
48	48 x 1 FIR compute clocks
2	FIR input sample writes
6	6 x 1 resampler compute clocks
1	Resampler input sample writes
1	Jump instruction
1	Wait instruction
105	Clock cycles per output

Total decimation is 8, so the input sample rate for the FIR chain could be up to:

$f_{CLK}/(ceil(105/8)) = f_{CLK}/14$.

With a 65MHz clock, this would support a maximum input sample rate to the FIR processor of 4.6MHz and an output sample rate up to 0.580MHz. The shaping filter impulse response length would be:

(95 x 2)/580,000 = 82µs.

The maximum output sample rate is dependent on the length and number of FIRs and their decimation factors.

Illustrating this concept with Filter Example #3, a higher speed filter chain might be comprised of one decimate-by-2 halfband filter (15 taps) followed by a 30 tap shaping FIR filter with no decimation. The program for this example could be:

SAMPLE FILTER #3 PROGRAM

STEP	INSTRUCTION
0	Wait for enough input samples (2 in this case)
1	FIR Type = even symmetry 19 taps Halfband Dec x 2 Compute one output Memory block size 32 Memory block start at 0 Coefficient block start at 18 Output to step 2 Reset wait count
2	FIR Type = even symmetry 30 taps Dec x 1 Compute one output Memory block size 64 Memory block start at 32 Coefficient block start at 64 Step size 1 Output to AGC
3	Jump, Unconditional, to 0

The number of clock cycles required to compute an output for Sample filter #3 is calculated as follows:

SAMPLE FILTER #3 CLOCK CYCLES CALCULATION

CLOCK CYCLES	FUNCTION PERFORMED
6	6 x 1 HBF compute clocks
2	HBF input writes
15	15 x 1 FIR compute clocks
1	1 FIR input write
1	1 wait
1	1 jump
26	Clock cycles per output

For Filter Example #3 and a 65MSPS input, the maximum output sample rate would be 2.5MSPS and the maximum FIR processor input sample rate would be 5MSPS (At 80MSPS, the FIR could be up to 42 taps).

Channels 0, 1, 2 and 3 can be combined in a polyphase structure for increased bandwidth or improved filtering.

Filter Example #4 will be used to demonstrate this capability.

Symbol rate of 4.096 MSym. The desired output sample rate is 8.192MSPS. Arrange the four back end sections as four filters operating on the same CIC output at a rate of

65.536MHz/4=16.384MHz.

Each channel computes the same sequence, offset by one output sample from the previous sample. Each channel decimates down to 2.048M and then the channels are

multiplexed together to get the desired 8.192MSPS. The input sample rate to the final filter of each channel must meet Nyquist for the final output to assure that no information is lost due to aliasing.

SAMPLE FILTER #4 PROGRAM

STEP	INSTRUCTION
0	Wait for enough input samples (8 in this case)
1	FIR type = even symmetry 44 taps decx8 compute one output memory block size 64 memory block start at 0 coefficient block start at 64 step size 1 output to AGC offset memory read pointers by 0, -2, -4, -6
2	Jump, Unconditional, to 0

The number of FIR taps available for these requirements is calculated as follows:

65536/2048 = 32 clocks

minus (8writes + 1wait + 1jump = 10clocks)

= 22 clocks

Therefore, the number of taps is:

22 x 2 = 44 taps.

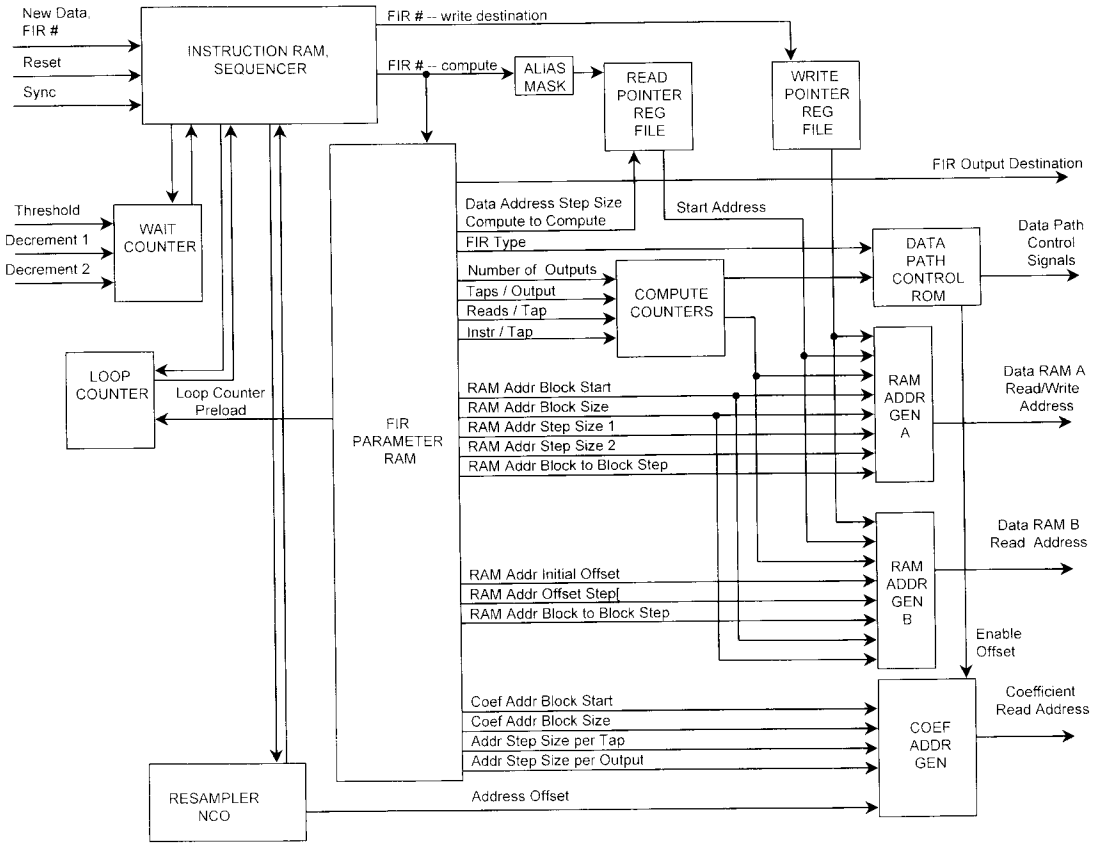
Multiplexing the four outputs gives a final output sample rate of 8.192.

The impulse response is 44 taps at 16.384M or 22 output samples (11 symbols at 4.096M).

The AGC loop filter output of channel 4 can be routed to control the forward AGC gain control of all four channels. This assures that the gains of the four back end sections are the same. The gain error, however, is only computed from every fourth output sample.

The back end processing sections of two or more HSP50216s can be combined using the same polyphase approach, but the AGC gain from one part cannot be shared with another part (except via the µP interface), so polyphase filter using multiple parts would typically usually use a fixed gain.

Filter Sequencer



The filter sequencer is programmed via an instruction RAM and several control registers. These are described below.

Instruction RAMs

The filter compute engine is controlled by a simple sequencer supporting up to 32 steps. Each step can be a filter or one of four sequence flow instructions - wait, jump (conditional or unconditional), load loop counter, or NOP. There are 128 bits per instruction word with each word consisting of condition code selects, FIR parameters and data routing controls. Not all of the instruction word bits are used for all instruction types. The actual sequencer instruction is only 9 bits. The rest of the bits are used for filter parameters or for the loop counter preload. Each sequence step is loaded in four 32-bit writes. The mapping of the bit fields for the instruction types is shown in the instruction bit field table that follows.

When the filter is reset, the instruction pointer is set to 31 (the last instruction step). The read and write pointers are initialized on reset, so a reset must be done when the channel is initialized or restarted.

A fixed offset can be added to the starting read address of the filter in one sequence step. This function is provided to offset the data reads of the filters in a polyphase filter bank - all filters in the bank will write the same data to the same RAM location. To offset the computations the RAM read address is offset.

The instruction word bits (127:0) are assigned to memory words as follows:

- 31:0 to destination C C C C 0 0 0 1 0 x x x x x 0 0
- 63:32 to destination C C C C 0 0 0 1 0 x x x x x 0 1
- 95:64 to destination C C C C 0 0 0 1 0 x x x x x 1 0
- 127:96 to destination C C C C 0 0 0 1 0 x x x x x 1 1

where CCCC is the channel number and xxxxx is the instruction sequence step number. Note the µPHold bit in the filter compute engine control register (IWA = *00Ah) must be set for the microprocessor to read from or write to the instruction or coefficient RAMs.

Instruction Bit Fields

INSTRUCTION BIT FIELDS

BIT POSITIONS	FUNCTION	DESCRIPTION
8:0	Instruction	Instruction Field Bit Mapping Bit 8 7 6 5 4 3 2 1 0 Type WAIT 0 0 X X X X C C C FIR 0 1 Start IncrRS DecrSel DecrEn LdLp DecrLp EnU/C JUMP 1 J J J J J C C C (NOPs and loading the loop counter are special cases of the FIR instruction) XXXX = ignored JJJJJ = jump destination (sequence step number) CCC = condition code 000 = ($\overline{\text{waitcount} \geq \text{threshold}}$) 001 = waitcount ≥ threshold 010 = loop counter ≠ 0 011 = loop counter = 0 100 = $\overline{\text{RSCO}}$ Tab (RSCO - resampler NCO carry output) 101 = RSCO 110 = sync (if enabled) or µP controlled bit 111 = always Start = load parameters and start filter computation, set to zero for no-ops, loop counter loads IncrRS = increment resampler during this filter. Increments on start or at each FIR output depending on µPcontrol bit. DecrSel = selects between two decrement values for the wait counter. DecrEn = decrement wait count on starting this instruction. LdLp = load loop counter with the data in the I(20:9) bit field. The start bit should not be set when this bit is set. DecrLp = decrement loop counter on starting this instruction. EnU/C = enable U/C counter with this FIR. This multiplies the data by 1, j, -1, -j. The multiplication factor changes each time the filter runs.
14:9	FIR Type	FIR Parameter Bit Fields 14:9 FIR type 000000 NOP 000001 Decimating FIR, Even Symmetric, Even # Taps 000010 Decimating FIR, Even Symmetric, Odd # Taps 000011 Decimating FIR, Odd Symmetric, Even # Taps 000100 Decimating FIR, Odd Symmetric, Odd # Taps 000101 Decimating FIR, Asymmetric 001000 Resampling FIR, Asymmetric 001001 Interpolating HBF 100000 Decimating FIR, Complex (Asymmetric) NOTES: 1. Regular interpolation FIRs are successive runs of a FIR with no data address increment, but with coefficient start address increments. 2. Decimating HBFs are even symmetric, odd number of taps but with different data step sizes. 3. U/C FIR is a normal FIR with the U/C bit enabled. 4. Other codes may be added in the future.
17:15	Steps per FIR	Specifies the number of steps per FIR instruction sequence (load with value minus 1) (set to 0 for all FIR types except complex which is set to 1)

INSTRUCTION BIT FIELDS (Continued)

BIT POSITIONS	FUNCTION	DESCRIPTION
28:18	Destination	Destination Field Bit Mapping 28 27 26 25 24 23 22 21 20 19 18 AGCLFGN AGCLF Path1 Path0 OS FB F4 F3 F2 F1 F0 AGCLFGN AGC loop gain select. Only applies to Path 1. Loop gain 0 or 1 if AGCLF bit is set. Set to 0 (1 is a test mode for future chips). AGCLF AGC loop filter enable. Only applies to Path 1.The AGC loop is updated with the magnitude of this sample (Path(1:0) = 01). Path(1:0) Back End Data Routing Path Selection 00 Route output back to filter compute engine input to another FIR in the filter chain. 01 Route output thru the FIFO and AGC forward path to the cartesian-to-polar coordinate converter conversion and output (I1, Q1, magnitude, phase, gain) and also to route to a discriminator (i.e., $d\phi/dt$ FIR). 10 Route output directly to the output, bypassing the FIFO and AGC (I2, Q2). This path also routes to next channel FIR input. OS Enable output strobe. Setting this bit generates a data ready signal when the data reaches the output section and starts the serial output sequence (paths 1, 2, 3). If OS is not set, there will be no output to the outside world from this channel, for that output calculation, but the data will be loaded into its output holding register (OS would not be set when routing the data to another back end when cascading channels). FB Feedback data path. When set, the magnitude and phase from the cartesian-to-polar coordinate converter block are routed to the filter compute engine input. Provided for discriminator filtering. F(4:0) Filter select. For data recirculated to the input of the FIR processor by path 0 or from the cartesian to polar coordinate converter output, these bits tell which filter sequencer step gets it as an input.
31:29	Round Select	31:29 Round Select (Add rounding bit at specified location) 000 2^{-24}, use this code when downshifting is not used. 001 2^{-23} 010 2^{-22} 011 2^{-21} 100 2^{-20} 101 2^{-19} 110 2^{-18} 111 no rounding Provided for use with the coefficient down-shift bits.
41:32	Data Memory Block Start	Memory block base address, 0-1023, 0-383 are valid for the HSP50216.
44:42	Data Memory Block Size	44:42 Block Size 0 8 1 16 2 32 3 64 4 128 5 256 6 512 7 1024 (modulo addressing is used)
52:45	Data Memory Block-to-Block Step	0-255, usually equal to the decimation factor for the FIR in this instruction.

INSTRUCTION BIT FIELDS (Continued)

BIT POSITIONS	FUNCTION	DESCRIPTION
62:53	Coefficient Memory Block Start	Memory base address of coefficients, 0-1023, 0-511 are valid on the HSP50216.
63	Reserved	Set to 0
66:64	Coefficient Memory Block Size	66:64 Memory Block Size 0 8 1 16 2 32 3 64 4 128 5 256 6 512 7 1024 (Modulo addressing can be used, but is usually not needed. If not needed this bit field can always be set to 7).
75:67	Number of FIR Outputs	Number of FIR outputs (range is 1 to 512, load w/ desired value minus 1). This is usually equal to the total decimation that follows the filter.
84:76	Read Address Pointer Step	Read address pointer step (for next run). This is usually equal to the filter decimation times the number of outputs from the instruction.
93:85	Initial Address Offset	Initial address offset (to ADDRB). This is the offset from the start address to other end of filter. For symmetric filters, usually equal to -1 x (number of taps -1).
95:94	Reserved	Set to 0
104:96	Memory Reads Per FIR Output	This is based on the number of taps (load with value below minus 1). Type — Value Symmetric, even number of taps — (taps/2) or floor((taps+1)/2) Symmetric, odd number of taps — (taps+1)/2 or floor((taps+1)/2) Decimating HBF — (taps+5)/4 Asymmetric — taps Complex — taps Resampling — taps/phase (six taps per phase for the ROM'd coefficients provided) Interpolating HBF — (taps+5)/4-1
106:105	Clocks Per Memory Read	Set to 0 for all but complex FIR, which is set to 1.
115:107	Data Memory Step Size 1	(ADDRA) Step size for all but the last tap computation of the FIR. Set to -2 for HBF, -1 otherwise.
117:116	Data Memory Step Size 2	(ADDRA) Step size for last tap computation. Set to -1. 117:116 Step size 0 0 1 -1 2 -2 3 step size value
119:118	Data Memory Address Offset Step	(ADDRB) Step size for opposite end of symmetric filter. Set to +2 for Decimating HBF, to +1 for others (the B data is not used for asymmetric, resampling, and complex filters).

INSTRUCTION BIT FIELDS (Continued)

BIT POSITIONS	FUNCTION	DESCRIPTION
122:120	Coefficient Memory Step Size	(ADDRC) Usually set to 1. 122:120 Step size 0 0 1 1 2 2 3 4 4 8 5 16 6 32 7 64
125:123	Coefficient Memory Block-to-Block Step	(ADDRC) Usually set to 0. 125:123 Step size 0 0 1 1 2 2 3 4 4 8 5 16 6 32 7 64
127:126	Reserved	Set to 0

Basic Instruction Set

1. Wait for number of input samples $\geq$ threshold
   127:9 = 0
   8:0 = 001
   0000,0000,0000,0001h
2. Jump unconditional
   127:9 = 0
   8:0 = 1JJJJJ111b
   example: jump to step 0= 0000,0000,0000,0107h
3. Jump RSCO (jump on resampler NCO carry output)
   127:9 = 0
   8:0 = 1JJJJJ101b
   example: jump RSCO, step 0= 0000,0000,0000,0105h
4. Jump $\overline{\text{RSCO}}$ (jump on no resampler NCO carry output)
   127:9 = 0
   8:0 = 1JJJJJ100b
   example: jump $\overline{\text{RSCO}}$, step 0 = 0000,0000,0000,0104h
5. NOP single clock
   127:9 = 0
   8:0 = 010000000b
   NOP1 = 0000,0000,0000,0080h
6. Load Loop Counter
   127:21 = 0
   20:9 = Loop counter preload (tested against 0)
   8:0 = 010000100b
   example: LdLpCntr 14 = 0000,0000,0000,1C84h
7. NOPs more than 1 clock period
   NOP
8. FIR examples
   even#taps, odd#taps, even/odd symmetry, asymmetric, complex, hbf, interpolation, interpolation hbf, resampler, u/c

Single FIR Basic Program

This is the basic program for a single FIR. This program applies to decimation filters (including DECx1) that are symmetric or asymmetric (but not complex). The FIR output is routed through path A with the AGC enabled.

0 - WAIT FOR ENOUGH SAMPLES

0000	0000	0000	0000	0000	0000	0000	0000	127:96	00000000h
0000	0000	0000	0000	0000	0000	0000	0000	95:64	00000000h
0000	0000	0000	0000	0000	0000	0000	0000	64:32	00000000h
0000	0000	0000	0000	0000	0000	0000	0001	31:0	00000001h

1 - FIR

0000	0001	0101	1111	1111	100R	RRRR	RRRR	127:96	015FF---h
00TT	TTTT	TTTD	DDDD	DDDD	0000	0000	0111	95:64	-----007h
0000	1000	0000	0000	0000	1010	0000	0000	63:32	08000A00h
0000	1011	0000	0000	0FFF	FFF0	1100	1000	31:0	0B00--C8h

2 - JUMP TO STEP 0

0000	0000	0000	0000	0000	0000	0000	0000	127:96	00000000h
0000	0000	0000	0000	0000	0000	0000	0000	95:64	00000000h
0000	0000	0000	0000	0000	0000	0000	0000	64:32	00000000h
0000	0000	0000	0000	0000	0001	0000	0111	31:0	00000107h

Four bit fields must be filled in:

F - filter type (this example applies to types 1-5)
D - decimation (also loaded into wait threshold)
T - number of taps minus 1
R - clocks/calculation (=floor((taps+1)/2) for symmetric, = taps for asymmetric)

The rest of the instruction RAM would typically be filled with NOP instructions:

0000	0000	0000	0000	0000	0000	0000	0000	127:96	00000000h
0000	0000	0000	0000	0000	0000	0000	0000	95:64	00000000h
0000	0000	0000	0000	0000	0000	0000	0000	64:32	00000000h
0000	0000	0000	0000	0000	0000	1000	0000	31:0	00000080h

Wait Preload Register

This register holds the wait counter threshold and two wait counter decrement values. Each is 10 bits. The wait counter counts filter input samples until the count is greater than or equal to the threshold. The wait counter then asserts a flag to the filter compute engine.

The wait counter threshold is typically set to the total number of input samples needed to generate a filter output. A "WAIT" instruction in the filter compute engine waits for the wait counter flag signal before proceeding. The filter compute engine would then compute all the filters needed to produce an output and then would jump back to the "WAIT" instruction.

The wait counter is implemented with an accumulator. This allows the count to go beyond the threshold without losing the sample count. Two bits in the FIR instruction decrement the wait counter (subtract a value) and select the decrement value. The decrement value is typically the number of samples needed for an output (total decimation), though it can be a different value to ignore inputs and shift the timing. (The read pointer increment must be adjusted as well.)

The filter compute engine sequencer does not count each input sample or track whether each filter is ready to run. Instead, the wait counter is used to determine whether there are enough input samples to compute all the filters in the chain and get an output sample from the entire filter chain. This adds some additional delay since intermediate results are not precalculated, but it simplifies the filter control. The number of samples needed is equal to the total decimation of the filter chain. For example, with two decimate-by-2 halfband filters and a decimate-by-2 shaping FIR, the total decimation would be 8 so 8 samples are needed to compute an output. HBF1 would compute four times to generate four inputs to HBF2. HBF2 would compute twice to generate the two samples that the shaping FIR needs to compute an output.

Resampler NCO

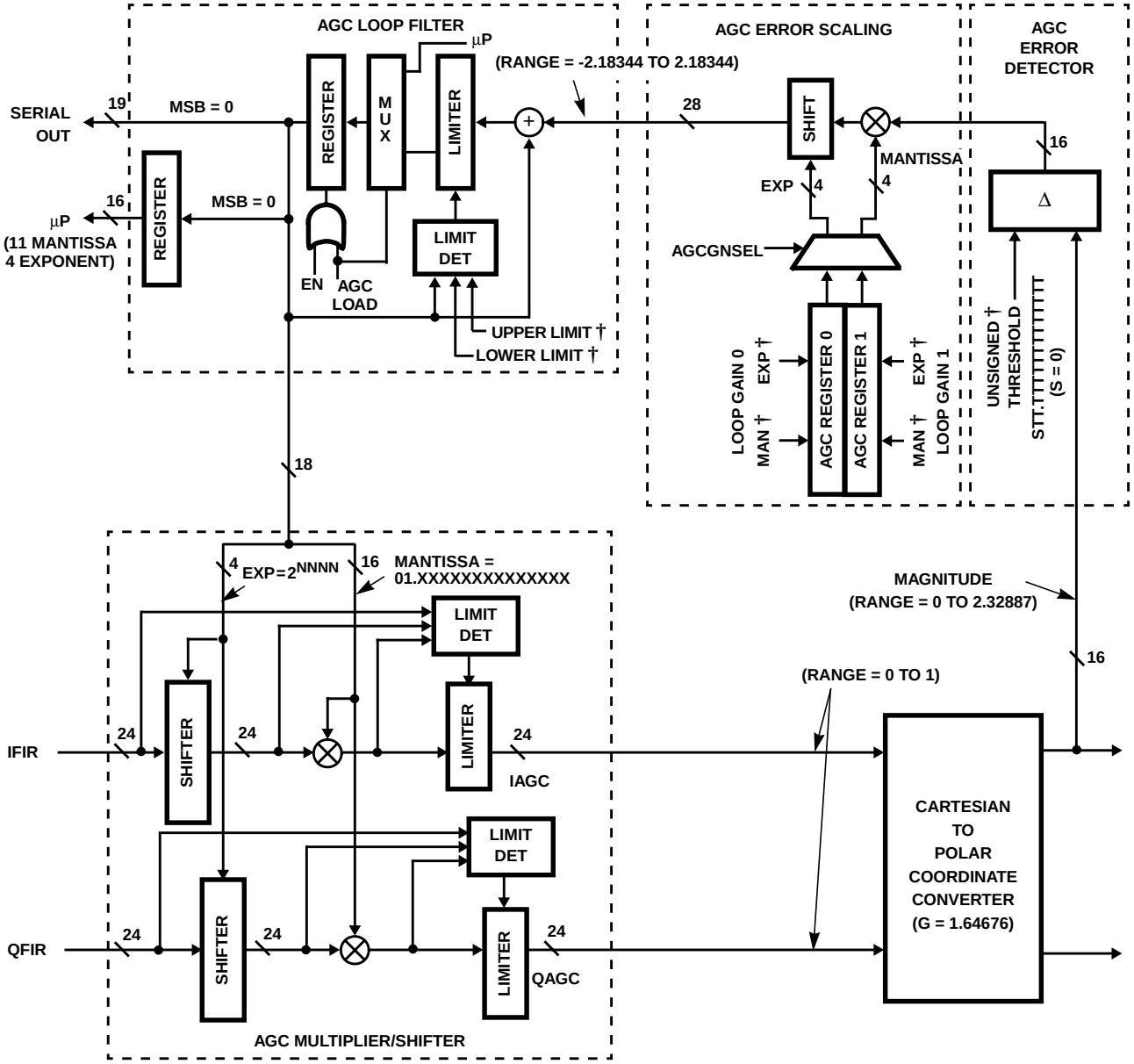
The NCO is incremented by the filter compute engine. A bit in the filter instruction selects whether the NCO is incremented for that filter output. The center frequency control is double buffered, i.e., the control word is written to one register via the µP interface and then transferred to another (active) register on a write to the TNCF update strobe location or on a SYNCI (if enabled).

As it is not possible to represent some frequencies exactly with an NCO and therefore, phase error accumulates eventually causing a bit slip, the phase accumulator length has been sized to where the error is insignificant. At an update rate of 1MHz, half an LSB of error in loading the 56-bit accumulator is 7e-12. After 1 year, the accumulated phase error is only 0.2e-3 of a bit (<1/10 of a degree).

The NCO update by the filter compute engine is typically at the resampler's input rate. The NCO then rolls over at a fraction of the resampler input rate. The output frequency is:

$(f_{IN}/2^{56})*N$.

N should be between 40000000000000h and FFFFFFFFFFFFFFh (decimation from 1 to 4). The resampler changes the sample rate by computing an output or not at each input. If an output is computed, its phase is shifted based on the NCO phase to slowly slide the timing of the output relative to the input. The output of the part will be at the input sample boundaries (except for any FIFOing following the filter compute engine). If D/A converted directly, there would be artifacts from the uneven sample spacing, but if the samples are stored and reconstructed at the proper rate (the NCO rollover rate), the signal would have only the distortion produced by interpolation image leakage and the time quantization due to the limited number of interpolation filter phases (32).



† Controlled via microprocessor interface.

FIGURE 1. AGC FUNCTIONAL BLOCK DIAGRAM

AGC

The loop gain register values adjust the response/settling time of the AGC loop. There are four values in two sets. Each set has both an attack and a decay gain. This allows asymmetric adjustment for applications such as VOX systems where the signal turns on and off. In these applications, the gains would be set for fast attack and slow decay so that the part decreases the gain quickly when the signal turns on, but increases the gain slowly when the signal turns off (in anticipation of it turning back on shortly).

Setting both the attack and decay gain values to zero disables the AGC (sets it as programmable gain stage).

The loop gains are floating point with a 4-bit mantissa (0.MMMM) and 4-bit exponent (2^{EEEE}). The gains through the AGC are:

	3	3	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1													
2^	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0	
	3	2	1	0	1	2	3	4	5	6	7	8	9	0	1	2	3																
Gain Error	S	S	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	(threshold - magnitude)															
																		S = 0 if mag < or = to thresh															
																		S = 1 if mag > thresh															
																		in median mode, the error is set to															
																		SS10000000000000 (±2.0)															
																		1 110000000000000															
																		0 010000000000000															
Mant mult out	S	S	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X	X												
$x2^{-17}$	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	X	X	X	X	X	X	X	X	X	X	X	X	
EXP = 0	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	X	X	X	X	X	X	X	X	X	X	X	X	
EXP = 1	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	X	X	X	X	X	X	X	X	X	X	X	X	0	
EXP = 2	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	X	X	X	X	X	X	X	X	X	X	X	X	0	0	
EXP = 4	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	S	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0		
EXP = 8	S	S	S	S	S	S	S	S	S	S	S	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0		
EXP = 15	S	S	S	S	S	X	X	X	X	X	X	X	X	X	X	X	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0		
UL, LL	(0)	E	E	E	E	M	M	M	M	M	M	M	M	M	M	M																	
LOAD	(0)	E	E	E	E	M	M	M	M	M	M	M	M	M	M	M																	
READ (µP)	0	E	E	E	E	M	M	M	M	M	M	M	M	M	M	M																	
OUTPUT	0	E	E	E	E	M	M	M	M	M	M	M	M	M	M	M	M	M	M		TBD												
FORWARD GAIN		E	E	E	E	M	M	M	M	M	M	M	M	M	M	M	M	M	M														

The forward gain consists of a 4-bit exponent and 14-bit mantissa and an implied 1 for an overall gain of:

0 1.M M M M M M M M M M M M M M * 2^{EEEE}.

The gain weighting in dB is approximately:

E	E	E	E	M	M	M	M	M	M	M	M	M	M	M	M	M	M
4	2	1															
8	4	2	6	3	1.	0.	0.	0.	0.	0.	0.	0.	0.	0.	0.	0.	0.
					5	7	3	1	0	0	0	0	0	0	0	0	0
						5	7	8	9	4	2	1	0	0	0	0	0
							5	7	3	6	3	1	5	2	1	0	0
								5	8	9	4	7	9	9	5	7	4

For a full scale error, the minimum non-zero AGC slew rate would be approximately 0.0002dB/output or 20dB/sec at 100ksps. The maximum gain would be 6dB/output. This much gain would probably result in significant AM on the output.

For median mode, the maximum gain step is approximately. 3dB/output. The step is fixed (it does not decrease as the error decreases) so a large gain will cause AM on the output at least that large. The gain should be lowered after the settling.

The AGC gain limits register sets the minimum and maximum limits on the AGC gain. The total AGC gain range is 96dB, but only a portion of the range should be needed for most applications. For example, with a 16-bit output to a processor, the 16 bits may be sufficient for all but 24dB of the total input range possible. The AGC would only need to have a range of 24dB. This allows faster settling and the AGC would be at its maximum gain limit except when a high power signal was received. The AGC may be disabled by setting both limits to the same value.

The limits are on the forward gain are mapped as:

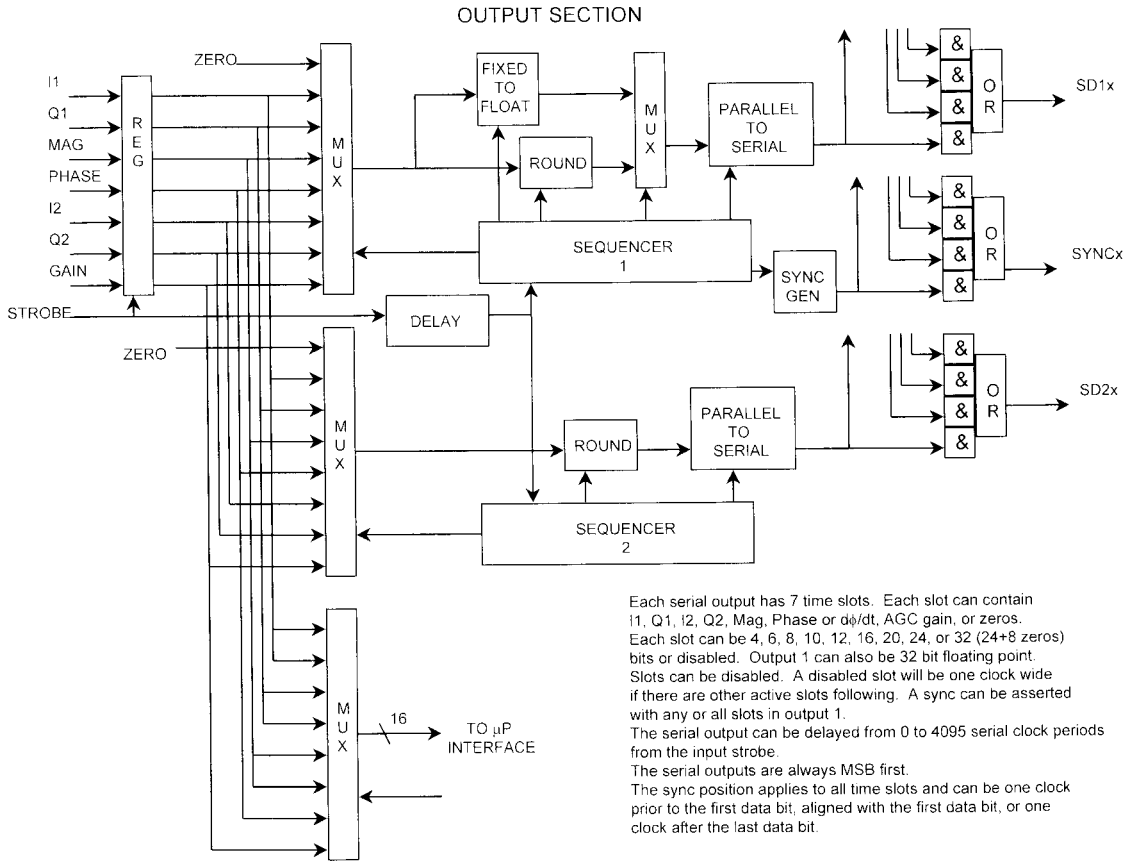
	E	E	E	E	M	M	M	M	M	M	M	M	M	M	M	M
(	0	1.	M	M	M	M	M	M	M	M	M	M	M	M	*	2^{EEEE})

The AGC loop adjusts its gain to maintain the output signal magnitude at a level proportional to this set point. There is a gain of 1.64676 in the I/Q to magnitude computation, so the threshold should be set to 0.82338 times the desired I/Q magnitude at the output of the part.

Output (I or Q)			0.	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	-1.0 to <1.0
Magnitude		Z	0.	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	0 to 1.414
Computed Mag	Z	1	0.	1	2	3	4	5	6	7	8	9	0	1	2	3	4	5	0 to 2.329
Threshold	2	1	0.	1	2	3	4	5	6	7	8	9	0	1	2	3			0 to 2.329*
Gain Error	S 2	1	0.	1	2	3	4	5	6	7	8	9	0	1	2				±2.329

* set MSB to zero.

Serial Data Output Formatter Section



Serial Data Output Control Register

The serial data output control register contains sync position and polarity (SYNCA, B, C or D), channel multiplexing, and scaling controls for the SD1x and SD2x (x = A, B, C or D) serial outputs (see Microprocessor Interface Section, Table 21, IWA *014h).

Channel Routing Mask

The multiplexing mask bits for each channel (see Microprocessor Interface Section Table 21, IWA *014h bits 19:16 for SD1x or bits 15:12 for SD2x) can be used to enable that channel's output to any of the four serial outputs. These bits control the AND gates that mask off the channels, so a zero disables the channel's connection to that output.

To configure more than one channel's output onto a serial data output, the SD1 serial outputs and syncs from each channel (0,1, 2 and 3) are brought to each of the SD1 serial output sections and the SD2 serial outputs are brought to each of the SD2 serial output sections (the syncs are only associated with the SD1 serial ouputs). There, the four outputs are AND-ed with the multiplexing mask programmed in the serial data output control registers of channels 0 thru 3 and OR-ed together. By gating off the channels that are not wanted and delaying the data from each desired channel appropriately, the channels can be multiplexed into a common serial output stream. It should be noted that in order to multiplex multiple channels onto a single serial data stream the channels to be multplexed must be synchronous.

Serial Data Output Time Slot Content/Format Registers

These four registers are used to program the content and format of the serial data output sequence time slots (see Microprocessor Interface Section, Tables 22 - 25, IWA *015h - *018h). There are seven data time slots that make up a serial data output stream. The number of data bits and data format of each slot is programmable as well as whether there will be a sync generated with the time slot (the syncs are only associated with the SD1 serial ouputs). Any of seven types of data or zeros can be chosen for each time slot. Eight bits are used to specify the content and format of each slot.

As an example, suppose we wanted to output 32-bit I and Q values from channels 0 and 1 into the SD1A serial data output stream, we would program the following settings in the channel's serial data output control and content/format registers:

Channel 0:

delay = 0 (IWA = 0014h, bits 11:0);

first data time slot = I, 32-bit (IWA = 0015h, bits 7:0);

second data time slot = Q, 32-bit (IWA = 0015h, bits 15:8);

third through seventh data time slot = zero and no sync,(IWA = 0015h, bits 31:16 and IWA = 0016h, bits 31:0);

enable the serial output for this channel in the serial routing mask (IWA = 0014h, bit 16).
Channel 1:

delay = 64(IWA = 1014h, bits 11:0);

first data time slot = I, 32-bit (IWA = 1015h, bits 7:0);

second data time slot = Q, 32-bit (IWA = 1015h, bits 15:8);

third through seventh data time slot = zero and no sync, (IWA = 1015h, bits 31:16 and IWA = 1016h, bits 31:0);

enable the serial output for this channel in the serial routing mask (IWA = 1014h, bit 16).

The syncs for the I and Q data are programmed as desired. The resulting order is CH0I first, then CH0Q, CH2I, and CH2Q.

As an example when no multiplexing of channel data is desired:

IWA = 0014h, bit 12 for channel 0 would be set;

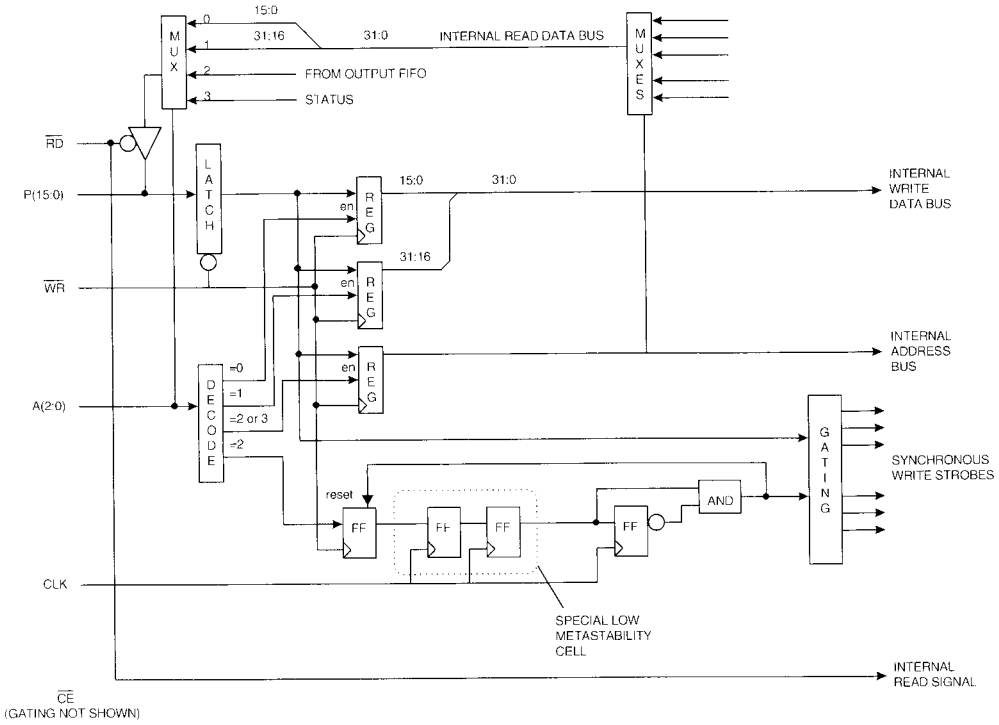
IWA = 1014h, bit 13 in channel 1 would be set;

IWA = 2014h, bit 14 in channel 2 would be set, and

IWA = 3014h, bit 15 in channel 3 would be set

allowing four serial data streams to be output on SD2A, SD2B, SD2C, and SD2D. The other bits in each channel's mask would be cleared (programmed to 0).

Microprocessor Interface



The HSP50216 Microprocessor (µP) interface consists of a 16-bit bidirectional data bus, P(15:0), three address pins, ADD(2:0), a write strobe ($\overline{WR}$), a read strobe ($\overline{RD}$) and a chip enable ($\overline{CE}$). Indirect addressing is used for control and configuration of the HSP50216. The control and configuration data to be loaded is first written to a 32-bit holding register at direct (external) addresses ADD(2:0) = 0 and 1, 16 bits at a time. The data is then transferred to the target register, synchronous to the clock, by writing the indirect (internal) address of the target register to direct (external) address 2, ADD(2:0) = 2. The interface generates a synchronous one clock cycle wide strobe to transfer the data contained in the holding register to the target register. The synchronization and write process requires 4 clock periods. New data **should not** be written to the holding register until after the synchronization period is over.

Data reads can be direct, indirect or FIFO-like depending on the data that is being read. The status register is read directly at direct (external) address 3, ADD(2:0) = 3. Readback of internal registers and memories is indirect. The 16-bit indirect (internal) address of the desired read source is first written to direct (external) address 3, ADD(2:0) = 3, to select the data. The data can then be read at direct

(external) addresses ADD(2:0) = 0 and 1 (bits 15:0 at address 0 and 31:16 at address 1). The data types available via the indirect read are listed in the Tables of Indirect Read Address (IRA) Registers. (Note that the µPHold bit contained in the target register at Indirect Write Address (IWA) = *00Ah must be set to suspend the filter compute engine before the memories can be written to or read from.)

The HSP50216 output data from the four channels is available through the microprocessor interface as well as from the serial data outputs. A FIFO-like interface is used to read the output data through the microprocessor interface. When new output data is available, it is loaded into a FIFO in a user programmed order (for details on the programming order see Global Write Address (GWA) = F820h - F83Fh). It can then be read, 16 bits at a time, at direct address 2, ADD(2:0) = 2. At the end of each read, the FIFO counter is advanced to the next location. This allows a DMA controller to read all of the data with successive reads to a single direct address. No writes or other interaction is required. The FIFO counter is reset and reloaded by each interrupt signal, see GWA F802h. New data in the FIFO is also indicated in the status register located at direct address ADD(2:0) = 3 if a polled mode is preferred. The eight data types available, for each of the four channels, via this interface are: I(23:8), I(7:0)+8 Zeroes, Q(23:8), Q(7:0)+8 Zeroes, Mag(23:8), Mag(7:0)+8 Zeroes, Phase (15:0), and AGC (15:0). The upper bits of I, i.e., I(23:8), and Q, i.e., Q(23:8), are not rounded to 16 bits. This interface can read the data from all the channels that are synchronized. However, because a common FIFO is used and the FIFO is reset and reloaded by each interrupt, it cannot be used for asynchronous channels.

The direct address map for the microprocessor interface is shown in the Table of Microprocessor Direct Read/Write Addresses and the procedures for reading and writing to this interface are provided below. The bit field details for each indirect read and write address is provided in the Table of Indirect Read Address (IRA) Registers, Tables of Indirect Write Address (IWA) Registers (Tables 1 - 32) and Tables of Global Write Address (GWA) Registers (Tables 33 - 43).

µP Read/Write Procedures

To Write to the Internal Registers:

1. Load the indirect write holding registers at direct address ADD(2:0) = 0 and 1 with the data for the internal register (16 or 32 bits depending on the internal register being addressed).
2. Write the Indirect Write Address of the internal register being addressed to direct address ADD(2:0) = 2 (Note: A write strobe to transfer the contents of the Indirect Write Holding Register into the Target Register specified by the Indirect Address will be generated internally).
3. Wait 4 clock cycles before performing the next write to the indirect write holding registers.

To Write to the Internal Instruction/Coefficient RAMs:

1. Put the filter compute engine of the desired channel into the hold mode by setting bit 31 of the Filter Compute Engine / Resampler Control register located at IWA = *00Ah (Note: The * is equal to 0, 1, 2 or 3 depending on the channel being addressed). By setting bit 31 all FIR processing for the channel addressed will be stopped.
2. Load the indirect write holding registers at direct address ADD(2:0) = 0 and 1 with the data for the internal RAM location.
3. Write the Indirect Write Address of the internal RAM location being addressed to direct address ADD(2:0) = 2 (Note: A write strobe to transfer the contents of the Indirect Write Holding Register into the RAM location specified by the Indirect Address will be generated internally).
4. Wait 4 clock cycles before performing the next write to the indirect write holding registers.
5. After all data has been loaded, set the µPHold bit back low.

To Read Internal Registers:

1. Write the Indirect Read Address of the internal register being addressed to direct address ADD(2:0) = 3.
2. Perform a read of the Indirect Read Holding Registers at direct address ADD(2:0) = 0 and 1.

To Read Data Outputs:

1. Set up the µP FIFO Read Order Control Register (located at Global Write Address (GWA) = F820h - F83Fh).
2. Wait for interrupt or check flag.
3. Data can then be read, 16 bits at a time, at direct address 2, ADD(2:0) = 2.
4. Repeat step 3 for desired number of words.
5. Go to step 2.

To Read Instruction/Coefficient Values:

1. Put the filter compute engine of the desired channel into the hold mode by setting bit 31 of the Filter Compute Engine / Resampler Control register located at IWA = *00Ah (Note: The * is equal to 0, 1, 2 or 3 depending on the channel being addressed).
2. Write the Indirect Read Address (IRA) of the internal RAM/ROM location being addressed to direct address ADD(2:0) = 3.
3. Wait 4 clock cycles.
4. Read the data at direct address ADD(2:0) = 0 and 1.
5. After all the data has been read, set the µPHold bit back low.

TABLE OF MICROPROCESSOR DIRECT READ/WRITE ADDRESSES

<table>
<tr><th>ADD(2:0)</th><th>PINS</th><th>REGISTER DESCRIPTION</th></tr>
<tr><td>0</td><td>WR</td><td>Indirect Write Holding Register, Bits 15:0</td></tr>
<tr><td>1</td><td>WR</td><td>Indirect Write Holding Register, Bits 31:16</td></tr>
<tr><td>2</td><td>WR</td><td>Indirect Write Address Register for Internal Target Register (Generates a write strobe to transfer contents of the Write Holding Register into the Target Register specified by the Indirect Address, see also Tables of Indirect Address Registers)</td></tr>
<tr><td>3</td><td>WR</td><td>Indirect Read Address Register (Used to select the Read source of data - uses the same register as Direct Address 2 but generates a read strobe (for RAMs and AGC) as needed instead of a write strobe).</td></tr>
<tr><td>0</td><td>RD</td><td>Indirect Read, Bits 15:0</td></tr>
<tr><td>1</td><td>RD</td><td>Indirect Read, Bits 31:0</td></tr>
<tr><td>2</td><td>RD</td><td>Read Register (FIFO) - Reads FIFO data from output section (This location reads output data in the order loaded in Global Control Indirect Address Registers F820-F83F. The FIFO is automatically incremented to the next data location at the end of each read.)</td></tr>
<tr><td>3</td><td>RD</td><td>Status Register
<table>
<tr><th>P(15:0)</th><th>BIT DESCRIPTION</th></tr>
<tr><td>15:12</td><td>Unused</td></tr>
<tr><td>11:6</td><td>Read non-bus input pins ($\overline{ENIx}$, $\overline{RESET}$, SYNCI)</td></tr>
<tr><td></td><td>11 RESET (Note: This bit is inverted with respect to the RESET input pin)</td></tr>
<tr><td></td><td>10 $\overline{ENIA}$</td></tr>
<tr><td></td><td>9 $\overline{ENIB}$</td></tr>
<tr><td></td><td>8 $\overline{ENIC}$</td></tr>
<tr><td></td><td>7 $\overline{ENID}$</td></tr>
<tr><td></td><td>6 SYNCI</td></tr>
<tr><td>5:2</td><td>Mask revision number</td></tr>
<tr><td>1</td><td>Level detector integration done. Active high.</td></tr>
<tr><td>0</td><td>New FIFO output data available (used for polling mode vs interrupt mode) Active low</td></tr>
</table></td></tr>
</table>

Tables of Indirect Write Address (IWA) Registers

Note: These Indirect Write Addresses are repeated for each channel. In the addresses below, the ***** field is the channel select nibble. These bits of the Indirect Address select the target channel register for the data. Values of 0 through 3 and F are valid. A channel select nibble value of F is a special case which writes the data to the same location in each of the four channels simultaneously.

TABLE 1. CHANNEL INPUT SELECT/FORMAT REGISTER (IWA = *000h)

P(15:0)	FUNCTION
15:13	Channel Input Source Selection - Selects as the data input for the channel specified in the Indirect Address either A(15:0), B(15:0), C(15:0), D(15:0) or the µP Test Input register as shown below. 15:13 Source Selected 000 A(15:0) 001 B(15:0) 010 C(15:0) 011 D(15:0) 100 µP Test input register. This is provided for testing and to zero the input data bus when a channel is not in use. The Global Write Address register for the µP Test input register is F807h.
12	µP Test Register input enable selection 1 Bit 11 of this register is used as the input enable. 0 A one clock wide pulse generated on each write to lGWA F808h is used as the input enable. Select 0 to write test data into the part. Select 1 to input a constant or to disable the input for minimum power dissipation when an NCO/mixer/CIC section is unused.
11	µP input enable. When bit 12 is set, this bit is the input enable for the µP Test Register input. Active low. 0 Enabled 1 Disabled.
10	Parallel Data Input Format 0 Two's complement 1 Offset binary
9	Fixed/Floating point 0 Fixed point 1 Floating point. The 16-bit input bus is divided into mantissa and exponent bits grouped either 13/3 or 14/2 depending on bits 8 and 7. See text.
8:7	Floating point mantissa size select. The 16-bit data input is grouped as a 13/3 or 14/2 mantissa/exponent word. These control bits select the mantissa/exponent grouping, add an offset to the exponent and set the shift control saturation level. 00 11/3 bits 15:5 mantissa, 2:0 exponent 01 12/3 bits 15:4 mantissa, 2:0 exponent 10 13/3 bits 15:3 mantissa, 2:0 exponent 11 14/2 bits 15:2 mantissa, 1:0 exponent See the exponent tables contained in the Input Select/Format Block Section.
6:4	De-multiplex control. These control bits are provided to select a channel from a group of multiplexed channels. Up to 8 multiplexed data streams can be demultiplexed. These control bits select how many clocks after the $\overline{ENIx}$ signal to wait before taking the input sample. $\overline{ENIx}$ should be asserted for one clock period and aligned with the first channel of the multiplexed data set. For example, if four streams are multiplexed at half the clock rate, $\overline{ENIx}$ would align with the first clock period of the first stream, the second would start two clocks later, the next 4 clocks after $\overline{ENIx}$, etc. The samples are aligned with $\overline{ENIx}$ (zero delay) at the input of the NCO/Mixer/CIC stage at the next $\overline{ENIx}$. 000 Zero delay 111 7 clock periods of delay. All values from 0 through 7 are valid.

TABLE 1. CHANNEL INPUT SELECT/FORMAT REGISTER (IWA = *000h)

P(15:0)	FUNCTION
3	Interpolated/Gated Mode Select 0 Gated. The carrier NCO and CIC are updated once per clock when $\overline{ENIx}$ is asserted. 1 Interpolated. The CIC is updated every clock. The carrier NCO is updated once per clock when $\overline{ENIx}$ is asserted. The input is zeroed when $\overline{ENIx}$ is high.
2	Enable COF/COFSYNC inputs. When set, this bit enables two bits from the D(15:0) input data bus to be used as a carrier offset frequency input.
1	Enable SOF/SOFSYNC inputs. When set, this bit enables two bits from the D(15:0) input data bus to be used as a resampler offset frequency input.
0	Enable PN. When set, A PN code, weighted by the gain in location *001, is added to the input samples at the output of the mixer.

TABLE 2. PN GAIN REGISTER (IWA = *001h)

P(15:0)	FUNCTION
31:16	Reserved, set to all 0's.
15:0	PN generator gain register. This input is provided to reduce the sensitivity of the receiver. A PN code, weighted by the value in this location, is added to the data at the output of the mixer. Adding noise has the effect of increasing the receiver noise figure. One reason to do this would be to decrease the basestation cell size in small steps. This method is very accurate and repeatable and can be done on a FDM channel by channel basis. It does, however, reduce the overall dynamic range. An alternate way is to add attenuation at the RF and adjust the whole range upward. This does not reduce the overall range but only shift it, with the shift being done on all channels simultaneously.

TABLE 3. CIC DECIMATION FACTOR REGISTER (IWA = *002h)

P(15:0)	FUNCTION
15:0	Load with the desired CIC decimation factor minus 1.

TABLE 4. CIC DESTINATION FIR AND OUTPUT ENABLE/$\overline{DISABLE}$ REGISTER (IWA = *003h)

P(15:0)	FUNCTION
5:1	CIC output destination (FIR # in FIR processor). Usually set to 00001.
0	CIC output enable. Active high. When low, the data writes from the CIC to the filter compute engine are inhibited.

TABLE 5. CARRIER NCO/CIC CONTROL REGISTER (IWA = *004h)

P(15:0)	FUNCTION
31:19	Reserved, set to zero.
18:14	CIC barrel shift control. 00000 is the minimum shift factor and 11111 is maximum shift factor. This compensates for the CIC filter gain of R^N, where N is the number of enabled CIC stages and R is the CIC decimation factor. The equation used to compute the shift factor is: Shift Factor = 45 - Ceiling($\log_2(R^N)$). Examples: N R Shift Factor 5 512 0 5 8 30
13:9	CIC stage bypasses. The integrator/comb pairs are numbered 1 thru 5 with 1 being the first integrator and first comb. Bit 13 bypasses the first integrator/comb pair, bit 12 bypasses the second, etc. The first integrator is the largest. Typically, the stages are enabled starting with stage 1 for maximum decimation range.
8:6	Carrier phase shift. Phase shifts of N*(π/4), N = 0 to 7.
5	Clear feedback (test signal or for mixer bypass).
4	NCO clear feedback on load.
3	Update frequency on SYNCI. Redundant. Set to1. See GWA register F802h.

TABLE 5. CARRIER NCO/CIC CONTROL REGISTER (IWA = *004h) (Continued)

P(15:0)	FUNCTION
2:1	Number of Carrier Offset Frequency (COF) serial input bits. 00 8 01 16 10 24 11 32
0	Enable serial offset frequency (zeros the data already loaded via the COF/COFSYNC pins). To disable the COF shifting see IWA register *000h.

TABLE 6. CARRIER NCO CENTER FREQUENCY REGISTER (IWA = *005h)

P(15:0)	FUNCTION
31:0	Carrier Center Frequency (CCF) This is the frequency control for the carrier NCO. The center frequency control is double buffered. The contents of this register are transferred to the active register on a write to the CCFStrobe location or on a SYNCI (if load on SYNCI is enabled). The carrier center frequency is: CCF*$f_{CLK}/(2^{32})$. CCF is a twos complement number and has a range of -2^{31} to $(2^{31}-1)$. f_{CLK} is the input sample rate ($\overline{ENIx}$ assertion rate) for gated mode and the clock rate for interpolated mode.

TABLE 7. CARRIER NCO CENTER FREQUENCY UPDATE STROBE REGISTER (IWA = *006h)

P(15:0)	FUNCTION
N/A	Writing to this address generates a strobe that transfers the CCF value to the active frequency register. The transfer to the active register can also be done using the SYNCI pin to synchronize the transfer in multiple parts or to synchronize to an external event. The value in the active register can be read at this address (the center frequency control before the serially loaded offset value is added). To read the value, either write this address to A(1:0) = 11 and then read at A(1:0) = 00 and 01, or read the value at A(1:0) = 00 and 01 after writing to this address and before writing a new address to either A(1:0) = 10 or 11.

TABLE 8. TIMING NCO FREQUENCY CONTROL REGISTER, MSW (IWA = *007h)

P(15:0)	FUNCTION
31:0	These are the upper 32 bits of the 56-bit timing (resampler) NCO center frequency control.

TABLE 9. TIMING NCO FREQUENCY CONTROL REGISTER, LSW (IWA = *008h)

P(15:0)	FUNCTION
31:8	These are the lower 24 bits of the 56-bit timing (resampler) NCO center frequency control.
7:0	Unused, set to zero.

TABLE 10. TIMING NCO CENTER FREQUENCY LOAD STROBE REGISTER (IWA = *009h)

P(15:0)	FUNCTION
N/A for $\overline{WR}$ 31:0 for $\overline{RD}$	A write to this location will update the resampler NCO center frequency. The upper 32 bits of the active register can be read at this address.

TABLE 11. FILTER COMPUTE ENGINE/RESAMPLER CONTROL REGISTER (IWA = *00Ah)

P(15:0)	FUNCTION
31	µPHold. When set, this bit stops the filter compute engine and allows the µP access to the instruction and coefficient RAMs for reading and writing. On the high to low transition, the filter compute engine is reset (the read and write pointers are reset and the instruction at location 31 is fetched).
30	µPShiftZeroB. This bit, when set to zero, disables the coefficient shift bits (bits 9:8 of the master register when coefficient loading).
29	µPENLimit. This bit disables the data path saturation logic. Provided for test. Active high. Set to 0 to disable the normal ROM controlled limiting (ANDed with normal signal).

TABLE 11. FILTER COMPUTE ENGINE/RESAMPLER CONTROL REGISTER (IWA = *00Ah) (Continued)

P(15:0)	FUNCTION
28:24	µPZ(4:0). These bits, when set to zero, zero the corresponding read pointer address bits. This allows the pointers to be aliased, i.e., multiple filters can access and/or modify the same pointer. They are provided to change filters, coefficients or decimation over a sequence.
23	Unused, set to 0.
22	TCNO ENsync. If this bit is set, the center frequency is updated on a SYNCI. Redundant. Set to 1.
21:20	RSRVRS(1:0). Set to 01.
19	Beginning/$\overline{\text{End}}$. This bit selects whether the resampler NCO is updated at the beginning of a FIR computation or at the end of each FIR output computation. Usually, the resampler will be updated once at the beginning of each resampler computation and this will be bit set to 1. 1 Once at the beginning of the FIR instruction. 0 At the last tap of each of the instruction's FIR computations (once per output).
18	RSModeSelect. This bit selects whether the resampler is a phase shifter or a frequency shifter. 0 Phase shift. 1 Frequency shift.
17	RSCO. This bit is provided to force the resampler NCO carry when using the resampler as a phase shifter rather than for a frequency shift. This bit must be set for phase shifting and cleared for frequency shifting. (The bit is Or-ed with the normal carry.)
16	RS NCO clear phase accumulator feedback on load. When this bit is set, the feedback in the resampler NCO phase accumulator is zeroed whenever the center frequency word is updated. This forces the NCO to a known phase so the phase of multiple channels can be aligned.
15	Force NCO load. This bit, when set, zeroes the feedback in the resampler NCO phase accumulator. This is provided for test or to use the resampler for phase instead of frequency shifting.
14	Enable RS freq offset. This bit, when set, enables the serially loaded resampler offset frequency word. When zero, the offset is zeroed. To disable the shifting, see IWA register *000h.
13:12	Serial input word size. These bits select the number of bits in the resampler offset frequency word (loaded serially via SOF/SOFSYNC). 00 8 bits 01 16 bits 10 24 bits 11 32 bits
11:0	FIFODelay. A FIFO is provided at the output of the filter compute engine to smooth the sample spacing when using the resampler or interpolation FIRs. In these filters, the outputs can be produced in bursts or with gaps. The FIFO takes the samples in and outputs them based on a counter timeout. If the FIFO is empty and the counter is at its terminal count (hold state), the data is passed through and the counter is reloaded. If the counter is not at terminal count, the data is held in the FIFO until the counter times out. The FIFO can hold up to 4 samples. The delay is programmed in clock periods. The value programmed is one less than the number of clocks of delay. Set to 0 for a delay of one (fall through). The delay should be programmed to slightly less then the desired spacing to prevent overflow.

TABLE 12. FILTER START OFFSET REGISTER (IWA = *00Bh)

P(15:0)	FUNCTION
13:9	RAM Instruction number to which the offset is applied. 0-31. Aliasing applies. Used for polyphase filters.
8:0	Amount of offset. Offsets the data RAM address for filter #n. This is used to offset the channels from each other when breaking the processing up among multiple channels for polyphase filters. For example, four channels can receive the same data at 8 MSPS, filter and decimate by 8 to output at 1MHz. If the computations are offset by 2 samples each, then the outputs of the four channels can be multiplexed together to get an output sample rate of 4MSPS. With a 64MSPS clock, the composite filter could have more than 100 taps where a single channel would only be capable of around 24 taps at a 4MHz output. EXCEPT IN VERY RARE CIRCUMSTANCES, THIS VALUE SHOULD BE A NEGATIVE NUMBER.

TABLE 13. WAIT THRESHOLD/DECREMENT VALUE REGISTER (IWA = *00Ch)

P(15:0)	FUNCTION
31	µPTestBit. This bit is provided as a microprocessor controlled condition code for the filter compute engine for conditional execution or synchronous startup. Active high.
30	Set to 0.
29:20	Decrement value 1. Positive number.
19:10	Decrement value 0. Positive number. Usually set equal to the Threshold (bits 9:0).
9:0	Threshold. Number of samples needed to run a filter set and produce an output.

TABLE 14. RESET WRITE POINTER OFFSET REGISTER (IWA = *00Dh)

P(15:0)	FUNCTION
8:0	This parameter is the offset between filter compute engine read and write pointers on filter compute engine reset. On reset, the read and write pointers for all the filters are loaded, the read pointer with zero and the write pointer with this value. Set to zero for a single filter and two for a multi-filter chain.

TABLE 15. AGC GAIN LOAD REGISTER (IWA = *00Eh)

P(15:0)	FUNCTION
15:0	This location loads the AGC accumulator. If the loop attack/decay gain is set to zero and this value is within the AGC gain limits, the AGC will hold this value. If not, the AGC will be set to this gain (or to a limit) and then start to settle. 4xE (15:12), 12xM, (11:0)

TABLE 16. AGC GAIN READ STROBE REGISTER (IWA = *00Fh)

P(15:0)	FUNCTION
31:0 for $\overline{RD}$; N/A for $\overline{WR}$	Writing to this location will sample the AGC loop filter output (forward gain value) to stabilize it for reading. The value is read from this location after waiting the 4 clocks required for read synchronization. 31:16 AGC Gain for Channel 1. 15:0 AGC Gain for Channel 0.

TABLE 17. AGC LOOP ATTACK/DECAY GAIN VALUES REGISTER (IWA = *010h)

P(15:0)	FUNCTION
31:24	Loop gain 0, decay gain value (signal decay, increase gain) 31:28 = EEEE (exponent), 27:24 = MMMM (mantissa)
23:16	Loop gain 1, decay gain value 23:20 = EEEE (exponent), 19:16 = MMMM (mantissa)
15:8	Loop gain 0, attack gain value (signal arrival, decrease gain) 15:12 = EEEE (exponent), 11:8 = MMMM (mantissa)
7:0	Loop gain 1, attack gain value 7:4 = EEEE (exponent), 3:0 = MMMM (mantissa)

TABLE 18. AGC GAIN LIMITS REGISTER (IWA = *011h)

P(15:0)	FUNCTION
31:16	Upper gain limit. See AGC section.
15:0	Lower gain limit. See AGC section.

TABLE 19. AGC THRESHOLD REGISTER (IWA = *012h)

P(15:0)	FUNCTION
15:0	AGC threshold. Equals 1.64676 times the desired magnitude of the I1/Q1 output.

TABLE 20. AGC/DISCRIMINATOR CONTROL REGISTER (IWA = *013h)

P(15:0)	FUNCTION
10	µP AGC loop gain select.
9	Enable filter compute engine control of AGC loop gain. When this bit is set, a bit in the filter compute engine destination field selects which loop gain to use with that filter output's gain error. Setting bit 10 overrides this bit and forces a loop gain 1. 10:9 FUNCTION 00 Loop Gain 0 (µP controlled) 10 Loop gain 1 (µP controlled) 01 Loop Gain controlled by filter compute engine 11 Loop 1 (µP override of filter compute engine)
8	Mean/Median. This bit controls the settling mode of the AGC. Mean mode settles to the mean of the signal and settles asymptotically to the final value. Median mode settles to the median and settles with a fixed step size. This mode settles faster and more predictably, but will have more AM after settling. 1 Mean mode 0 Median mode
7:6	Unused. Set to zero.
5	PhaseOutputSel 1 dϕ/dt 0 Phase
4:3	DiscShift(1:0). Shifts the phase up 0, 1, 2, or 3-bit positions, discarding the bits shifted off the top. This makes the phase modulo 360, 180, 90, or 45 degrees to remove PSK modulation. The resulting phase is 18 bits.
2:0	DiscDelay(2:0). Sets the delay, in sample times, for the dϕ/dt calculation. 000 1 111 8

TABLE 21. SERIAL DATA OUTPUT CONTROL REGISTER (IWA = *014h)

P(15:0)	FUNCTION
28	Sync polarity 1 Active low (low for one serial clock per word with a sync). 0 Active high.
27:26	Reserved, set to zero.
25:24	Sync position. This applies to all time slots in the serial output. The Sync programming is associated with the SD1x serial output data stream (x = A, B, C, or D). 00 Sync is asserted during the clock period following the last data bit of the word (early sync). 01 Sync is asserted during the serial clock period prior to the first data bit of the serial word (late sync). 1X Sync is asserted during the serial clock period of the first data bit of the serial word (coincident sync).
23:22	Reserved, set to zero.

TABLE 21. SERIAL DATA OUTPUT CONTROL REGISTER (IWA = *014h) (Continued)

P(15:0)	FUNCTION
21:20	Magnitude output scale factor. The magnitude output of the cartesian to polar coordinate conversion has bits weighted as: $2^{(2\ 1\ 0.-1\ -2\ -3\ -4\ .\ .\ .)}$ The gain in the conversion is 0.82338. When using 16 bits, the range is such that the LSB has a weight of 0.00007 and the maximum output is 2.32, both after the conversion gain. This corresponds to an I/Q vector length of -83dBFS to +3dBFS. These control bits add gain (with saturation) for more resolution at the bottom of the scale. A code of 00 passes the magnitude unchanged, 01 shifts the magnitude up one bit position' 10 shifts by 2 positions and 11 shifts up three positions. The resulting bit weights and range (after conversion gain) for the unsigned numbers are: Code Bit Weights dBFS 00 2 1 0 -1 -2 . . . -11 -12 -13 +3 to -83 01 1 0 -1 -2 -3 . . . -12 -13 -14 +3 to -89 10 0 -1 -2 -3 -4 . . . -13 -14 -15 +1.7 to -95 11 -1 -2 -3 -4 -5 . . . -14 -15 -16 -4.3 to -101 The upper limits on codes 00 and 01 are the same, but 01 has no leading zero.
19:16	Serial data output SD1 routing mask. 0 disables. 1 enables. Bit Enabled Output 16 Enables the serial output for this channel to pin SD1A. 17 Enables the serial output for this channel to pin SD1B. 18 Enables the serial output for this channel to pin SD1C. 19 Enables the serial output for this channel to pin SD1D.
15:12	Serial data output SD2 routing mask. 0 disables. 1 enables. Bit Enabled Output 12 Enables the serial output for this channel to pin SD2A. 13 Enables the serial output for this channel to pin SD2B. 14 Enables the serial output for this channel to pin SD2C. 15 Enables the serial output for this channel to pin SD2D.
11:0	Output hold-off delay. This parameter adds additional delay from the output of the filter compute engine to start of the serial output stream for multiplexing channels. Load with the desired delay (0 = zero, 1 = one, 2 = two, etc.).

TABLE 22. SERIAL DATA OUTPUT 1 CONTENT/FORMAT REGISTER 1 (IWA = *015h)

P(15:0)	FUNCTION
31:24	Fourth serial slot in Serial Data Output 1 (SD1x). x = A, B, C or D. See bits 7:0 for functional description of bits 31:24.
23:16	Third serial slot in Serial Data Output 1 (SD1x). x = A, B, C or D. See bits 7:0 for functional description of bits 23:16.
15:8	Second serial slot in Serial Data Output 1 (SD1x). x = A, B, C or D. See bits 7:0 for functional description of bits 15:8.

TABLE 22. SERIAL DATA OUTPUT 1 CONTENT/FORMAT REGISTER 1 (IWA = *015h) (Continued)

P(15:0)	FUNCTION
7:0	First serial slot in Serial Data Output 1 (SD1x). x = A, B, C or D. Bit — Function 7 — Sync generated. When set, a sync pulse is generated with the data slot (Serial Data Output 1 only, i.e., the sync is only associated with Output 1). Set to zero for Output 2, SD2x. 6:3 — Word width/format. All fixed point data is twos complement. The data is rounded (asymmetrically, with saturation) to the desired number of bits. 0000 — 0-bit, fixed point (actually 1-bit position is used) 0001 — 4-bit, fixed point 0010 — 6-bit, fixed point 0011 — 8-bit, fixed point 0100 — 10-bit, fixed point 0101 — 12-bit, fixed point 0110 — 16-bit, fixed point 0111 — 20-bit, fixed point 1000 — 24-bit, fixed point 1001 — 32-bit fixed (8 LSBs are zeroed) 1010 — 32-bit, floating point, IEEE format All other codes are invalid. Note: Floating point format is only available on the Serial Data Output 1. Code 1010 is invalid on Serial Data Output 2. 2:0 — Data type 000 — Zeros 001 — I1 (data routed from FIFO and AGC path) 010 — Q1 (data routed from FIFO and AGC path) 011 — Magnitude of I1/Q1 100 — Phase (or dϕ/dt) of I1/Q1 101 — I2 (data routed directly from the filter processor) 110 — Q2 (data routed directly from the filter processor) 111 — AGC gain of I1/Q1 path The filter processor must be programmed appropriately to route the data to I1/Q1 or I2/Q2. NOTE: Disable a slot by setting the 8-bit word to 00h. When disabled, a slot still uses one clock period. If, for example, the slots are programmed to 16-bit, disabled, 16-bit, there would a one clock idle period between the two 16-bit data words. If a new data sample occurs before the current set of data has been output, the new data will preempt the output and the first slot of the new data will begin immediately. If a late sync was programmed, it will not occur. 0 1 2 3 4 5 6 7 8 9 A B C D E F 0 1 2 3 4 5 6 7 8 9 A B C D E F I,Q — 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 Z Z Z Z Z Z Z Z MAG — Z 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0 1 2 3 Z Z Z Z Z Z Z Z (MSB zero unless shifted) PH — 0 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 Z Z Z Z Z Z Z Z Z Z Z Z Z Z Z AGC — Z 1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 Z Z Z Z Z Z Z Z Z Z Z Z Z Z Z (MSB zeroed)

TABLE 23. SERIAL DATA OUTPUT 1 CONTENT/FORMAT REGISTER 2 (IWA = *016h)

P(15:0)	FUNCTION
31:24	Set to zero
23:16	Seventh serial slot in Serial Data Output 1 (SD1x). x = A, B, C or D. See bits 7:0 of Table 22 for functional description of bits 23:16.
15:8	Sixth serial slot in Serial Data Output 1 (SD1x). x = A, B, C or D. See bits 7:0 of Table 22 for functional description of bits 15:8.
7:0	Fifth serial slot in Serial Data Output 1 (SD1x). x = A, B, C or D. See bits 7:0 of Table 22 for functional description of bits 7:0.

TABLE 24. SERIAL DATA OUTPUT 2 CONTENT/FORMAT REGISTER 1 (IWA = *017h)

P(15:0)	FUNCTION
31:24	Fourth serial slot in Serial Data Output 2 (SD2x). x = A, B, C or D. See bits 7:0 of Table 22 for functional description of bits 23:16.
23:16	Third serial slot in Serial Data Output 2 (SD2x). x = A, B, C or D. See bits 7:0 of Table 22 for functional description of bits 23:16.
15:8	Second serial slot in Serial Data Output 2 (SD2x). x = A, B, C or D. See bits 7:0 of Table 22 for functional description of bits 15:8.
7:0	First serial slot in Serial Data Output 2 (SD2x). x = A, B, C or D. See bits 7:0 of Table 22 for functional description of bits 7:0.

TABLE 25. SERIAL DATA OUTPUT 2 CONTENT/FORMAT REGISTER 2 (IWA = *018h)

P(15:0)	FUNCTION
31:24	Set to zero
23:16	Seventh serial slot in Serial Data Output 2 (SD2x). x = A, B, C or D. See bits 7:0 of Table 22 for functional description of bits 23:16.
15:8	Sixth serial slot in Serial Data Output 2 (SD2x). x = A, B, C or D. See bits 7:0 of Table 22 for functional description of bits 15:8.
7:0	Fifth serial slot in Serial Data Output 2 (SD2x). x = A, B, C or D. See bits 7:0 of Table 22 for functional description of bits 7:0.

TABLE 26. SOFTWARE RESET REGISTER (IWA = *019h)

P(15:0)	FUNCTION
N/A	Writing to this location resets the following activities of the functional block indicated. Input Format/Select, NCO, Mixer and CIC Clears any pending enable in each channel's input demultiplexer function, loads the CIC decimation counter (the load value is indeterminate if the decimation counter preload register has not been loaded), clears all processing enables (stops all processing in the data path, but does not clear the data path registers). Filter Compute Engine Resets the Read/Write pointers, fetch instruction 31 and start the filter program execution. AGC Resets the compute blocks in both the forward and loop filter blocks (any calculations in progress are lost). Cartesian-to-Polar Coordinate Converter Resets the compute blocks (any calculations in progress are lost). FIFO Resets counter (clears the FIFO, all data is lost). Resampler Timing NCO Clears the slave (active) frequency registers and clears the phase accumulator. Output Section Resets the serial output section (clears all registers, counters, and flags but does not clear the configuration registers). Self Test Control Resets the self test control logic of the front end (Input Format/Select, NCO, Mixer, and CIC) and the back end (Filter Compute Engine, AGC, and Cartesian-to-Polar Coordinate Converter).

TABLE 27. CHANNEL TIMING ADVANCE STROBE REGISTER (IWA = *01Ah)

P(15:0)	FUNCTION
N/A	Writing to this location inserts one extra data sample in the CIC to FIR path by repeating a sample. Used for shifting the FIR filter compute engine timing.

TABLE 28. CHANNEL TIMING RETARD STROBE Register (IWA = *01Bh)

P(15:0)	FUNCTION
N/A	Writing to this location deletes one data sample in the CIC to FIR path. Used for shifting the FIR filter compute engine timing.

TABLE 29. FILTER COMPUTE ENGINE INSTRUCTION RAMS (IWA = *100h THRU *17Fh)

P(15:0)	FUNCTION
31:0	These locations in RAM are used to store the Filter Compute Engine instruction words. There are 128 bits per instruction word with each word consisting of condition code selects, FIR parameters and data routing controls. The filter compute engine is controlled by a simple sequencer supporting up to 32 steps where each step is defined by a 128 bit instruction word. The 128 bit instruction word is assigned to RAM memory in four 32 bit data writes through the Microprocessor Interface. Hence, 128 32-bit memory locations are required per channel to support the 32 steps of the Filter Sequencer. See the Filter Compute Engine and Filter Sequencer sections of the data sheet for more details.

TABLE 30. FILTER COMPUTE ENGINE INSTRUCTION POINTER RAMS (IWA = *180h THRU *1FCh)

P(15:0)	FUNCTION

TABLE 31. FILTER COMPUTE ENGINE COEFFICIENT RAM1 (IWA = *440h THRU *47Fh)

P(15:0)	FUNCTION
31:0	These locations in RAM are used to store the 22-bit filter coefficients used by the Filter Compute Engine of each channel in implementing a FIR filter. The 22-bit FIR filter coefficients are loaded in the upper 22 bits of each 32-bit RAM location. The two LSBs of the second byte (bits 9:8 of the total 32 bits, 31:0) are the shift bits. These are set to zero if not used. The least significant byte (bits 7:0 of the total 32 bits, 31:0) are ignored. RAM1 address space allows for storage of 64 filter coefficients out of the total of 192 filter coefficient storage locations. See the Filter Compute Engine and Filter Sequencer sections of the data sheet for more details.

TABLE 32. FILTER COMPUTE ENGINE COEFFICIENT RAM2 (IWA = *480h THRU *4FFh)

P(15:0)	FUNCTION
31:0	These locations in RAM are used to store the 22-bit filter coefficients used by the Filter Compute Engine of each channel in implementing a FIR filter. The 22-bit FIR filter coefficients are loaded in the upper 22 bits of each 32-bit RAM location. The two LSBs of the second byte (bits 9:8 of the total 32 bits, 31:0) are the shift bits. These are set to zero if not used. The least significant byte (bits 7:0 of the total 32 bits, 31:0) are ignored. RAM1 address space allows for storage of 128 filter coefficients out of the total of 192 filter coefficient storage locations. See the Filter Compute Engine and Filter Sequencer sections of the data sheet for more details.

Tables of Global Write Address (GWA) Registers

NOTE: These Global Write Addresses control global functions on the HSP50216, so they are not repeated for each channel. The top five address bits select this set of registers (F8XXh).

TABLE 33. TEST CONTROL REGISTER (GWA = F800h)

P(15:0)	FUNCTION
31:17	These bits can be routed to the output pins by setting bit 16 below. The bit to pin mapping is: 31 = Intrpt 30 = SYNCO 29 = SERCLK (unless x1 CLK is selected) 28 = SYNCA 27 = SYNCB 26 = SYNCC 25 = SYNCD 24 = SD1A 23 = SD1B 22 = SD1C 21 = SD1D 20 = SD2A 19 = SD2B 18 = SD2C 17 = SD2D This is provided for testing board level interconnects. To control the SERCLK output, a divided down clock must be selected in the serial clock control register (GWA = F803h).
16	This bit, when high, routes bits 31:17 to the output pins in place of the normal outputs. Bit 0 of this register must also be set to activate this function.
15:10	Unused - set to zero.
9	Set-up time to CLOCK adjust. Adjusting the delay trades set up time for hold time. This bit is used to best center the delay without a mask change.
8	Set-up time to WRITE adjust. Adjusting the delay trades set up time for hold time. This bit is used to best center the delay without a mask change.
7:4	These bits, when set, route the MSB of the SIN output of the channel's carrier NCO to the number 2 serial output pin in place of the normal output. 7=CH0 6=CH1 5=CH2 4=CH3
3	Offset I PN by XORing bit 10 of the PN generator with the output PN.
2	Enable (2^{23} - 1) PN generator. The PN signal that can be added to the mixer output of each channel is produced from a (2^{23} - 1) sequence, a (2^{15} - 1) sequence or both. Two separate generators are provided. The outputs of both are XORed together to extend the repeat period. Either or both generators can be disabled. The XORed output can further be XORed with a delayed version of the (2^{23} - 1) sequence on the I channel to decorrelate it from the Q channel. Otherwise, the same sequence will be used on both I and Q.
1	Enable (2^{15} - 1) PN generator.
0	Test mode. When asserted, this bit puts the chip into internal (self) test mode.

TABLE 34. BUS ROUTING CONTROL REGISTER (GWA = F801h)

P(15:0)	FUNCTION
31:24	Unused - set to zero.
23:20	Interrupt pulse width. The width of the interrupt pulse at the pin can be programmed to be from 1 to 15 clocks wide. Program with the desired number of clocks. (NOTE: The pulse counter is only reset with the RESET pin. If a channel is reset by software or a SYNCI, any interrupt pulse in process will finish.)
19:17	DataRdy delay (CH1 only). Test. From 1-8.
16	CH1orD# AGC to CH0 ext AGC. This bit selects whether the AGC loop filter output from CH1 or CH3 is routed to the external AGC gain input of CH0. 0=CH3, 1=CH1.
15:14	CH3 ext source mux sel. These bits select whether the CH2 source mux, CIC2, or FIR2out is routed to the external input of FIR3. 0=CH2srcmux, 1=FIR2, 2=CIC2.
13	CH2 ext source mux sel. This bit selects whether the CH1 external source mux or FIR1out is routed to the external input of FIR2. 0=CH1srcmux, 1=FIR1out.
12	CH1 ext source mux sel. This bit selects whether the CIC0 output or FIR0out is routed to the external input of FIRB. 0=CIC0, 1=FIR0out.
11	CH0 backend input sel. 0=CIC0, 1=CIC1 (test).
10	CH1 backend input sel 0=CIC1, 1=CH1 ext src mux.
9	CH2 backend input sel 0=CIC2, 1=CH2 ext src mux.
8	CH3 backend input sel 0=CIC3, 1=CH3 ext source mux.

TABLE 34. BUS ROUTING CONTROL REGISTER (GWA = F801h) (Continued)

P(15:0)	FUNCTION
7	CH0 Ext AGC input enable. 0=CH0 loop filt, 1=external input.
6	CH1 Ext AGC input enable 0=CH1 loop filt, 1=external input.
5	CH2 Ext AGC input enable 0=CH2 loop filt, 1=external input.
4	CH3 Ext AGC input enable Set to 0.
3	CH0 enable serial output 1=FIR0 out enabled to serial outputs.
2	CH1 enable serial output 1=FIR1 out enabled to serial outputs.
1	CH2 enable serial output 1=FIR2 out enabled to serial outputs.
0	CH3 enable serial output 1=FIR3 out enabled to serial outputs.

TABLE 35. RESET/SYNC/INTERRUPT SOURCE SELECTION REGISTER (GWA = F802h)

P(15:0)	FUNCTION
31	When set, an interrupt will be generated on each data output of channel 0 to the output block. Typically, this bit will only be set for one channel.
30	When set, the input to the part will be disabled (the input enable will be zeroed and held at zero) on a µP reset (this is always true for the reset pin, whether this bit is set or not, and additionally, the reset pin sets the input mode to gated). The input enable will be released for the input sample that aligns with the SYNCI signal. This is a method for starting up the processing synchronous with a particular data sample.
29	When this bit is set, the carrier center frequency will be updated from the holding register to the active register on SYNCI signals. If the bit is set in register IWA = *004h to clear the phase accumulator feedback on loading, this function will synchronize the phase of multiple channels. After initial synchronization, the bit in IWA = *004h can be cleared and updates will be synchronous and phase continuous across channels.
28	When this bit is set, the FIR filter compute engine is reset on SYNCI. Resetting the FIR filter compute engine requires 32 clock cycles to initialize the read and write pointers.
27	When this bit is set, the AGC is reset on SYNCI.
26	This bit has the same function as bit 29, but for the timing (resampler) NCO. The bit to zero the phase accumulator feedback is in register IWA = *00Ah.
25	When this bit is set, the CIC decimation counter is reset on SYNCI.
24	When this bit is set, the serial output block is reset on SYNCI. If bit 4 in location GWA F803h is set, the serial clock divider is also reset.
23:16	Same functions as 31:24 for channel 1.
15:8	Same functions as 31:24 for channel 2.
7:0	Same functions as 31:24 for channel 3.

TABLE 36. SERIAL CLOCK CONTROL REGISTER (GWA = F803h)

P(15:0)	FUNCTION
4	Enables resetting serial clock divider on SYNCI. When enabled, a SYNCI enabled for any of the serial data outputs in the Reset/Sync register will reset the serial clock divider.
3	SCLK polarity. 1 Clock low to high transition occurs at the center of the data bit. 0 Clock high to low transition at the center of the data bit.

TABLE 36. SERIAL CLOCK CONTROL REGISTER (GWA = F803h) (Continued)

P(15:0)	FUNCTION
2:0	SCLK rate. 000 Serial clock disabled. 001 Serial clock rate is Input CLK Rate. 010 Serial clock rate is Input CLK Rate/2. 011 Serial clock rate is Input CLK Rate/4. 100 Serial clock rate is Input CLK Rate/8. 101 Serial clock rate is Input CLK Rate/16. Other codes are undefined.

TABLE 37. INPUT LEVEL DETECTOR SOURCE SELECT/FORMAT REGISTER (GWA = F804h)

P(15:0)	FUNCTION
15:13	Channel Input Source Selection. Selects as the data input for the level detector either A(15:0), B(15:0), C(15:0), D(15:0) or the µP Test Input register as shown below. 15:13 Source Selected 000 A(15:0) 001 B(15:0) 010 C(15:0) 011 D(15:0) 100 µP Test input register. This is provided for testing and to zero the input data bus when a channel is not in use. The Top Level Control register address for the µP Test input register is F807h.
12	µP Register input enable select 1 = bit 11, 0 = one clock wide pulse on each write to location F808h. Select 0 to write data test data into the part. Select 1 to input a constant or to disable the input for minimum power dissipation when an NCO/mixer/CIC section is unused.
11	µP input enable. When bit 12 is set, this bit is the input enable for the µP register input. Active low. 0=enabled, 1=disabled.
10	Parallel Data Input Format 0 Two's complement 1 Offset binary
9	Fixed/Floating point 0 Fixed point 1 Floating point. The 16-bit input bus is divided into mantissa and exponent bits grouped either 13/3 or 14/2 depending on bits 8 and 7. See text.
8:7	Floating point mantissa size select. The 16-bit data input is grouped as a 13/3 or 14/2 mantissa/exponent word. These control bits select the mantissa/exponent grouping, add an offset to the exponent and set the shift control saturation level. 00 11/3 bits 15:5 mantissa, 2:0 exponent 01 12/3 bits 15:4 mantissa, 2:0 exponent 10 13/3 bits 15:3 mantissa, 2:0 exponent 11 14/2 bits 15:2 mantissa, 1:0 exponent
6:4	De-multiplex control. These control bits are provided to demultiplex an input data stream comprised of a set of multiplexed data streams. Up to 8 multiplexed data streams can be demultiplexed. These control bits select how many clocks after the $\overline{ENIx}$ signal to wait before taking the input sample. $\overline{ENIx}$ should be asserted for one clock period and aligned with the first channel of the multiplexed data set. For example, if four streams are multiplexed at half the clock rate, $\overline{ENIx}$ would align with the first clock period of the first stream, the second would start two clocks later, the next 4 clocks after $\overline{ENIx}$, etc. The samples are aligned with $\overline{ENIx}$ (zero delay) at the input of the NCO/Mixer/CIC stage at the next $\overline{ENIx}$. 000 zero delay 111 7 clock periods of delay.

TABLE 37. INPUT LEVEL DETECTOR SOURCE SELECT/FORMAT REGISTER (GWA = F804h) (Continued)

P(15:0)	FUNCTION
3	Interpolated/Gated Mode Select 0 Gated. The carrier NCO and CIC are updated once per clock when $\overline{ENIx}$ is asserted. 1 Interpolated. The CIC is updated every clock. The carrier NCO is updated once per clock when $\overline{ENIx}$ is asserted. The input is zeroed when $\overline{ENIx}$ is high.
2:0	Unused. Set to 0.

TABLE 38. INPUT LEVEL DETECTOR CONFIGURATION REGISTER (GWA = F805h)

P(15:0)	FUNCTION
21	1 Ones complement of 16-bit data after formatting. 0 Unmodified input.
20	1 Free run (ignore interval counter). 0 Stop when interval counter times out. This bit may also be set low temporarily when free running to stabilize the accumulator data for reading.
19:18	Input Level Detector Leak factor, A. 00 1 01 2^{-8} 10 2^{-12} 11 2^{-16}
17:16	Input Level Detector Mode 00 Leaky integrator ($Y_n = A*X_n + (1-A)*Y_{n-1}$, where A is the gain selected in bits 19:18). 01 Peak detector. 10 Integrator (bit 20 should be set to 0).
15:0	Input Level Detector Interval Load with two less than the desired number of input samples. The interval range is 2 to 65537 input samples.

TABLE 39. INPUT LEVEL DETECTOR START STROBE REGISTER (GWA = F806h)

P(15:0)	FUNCTION
N/A	Writing to this location clears the input level detector accumulator and restarts the interval counter. When the interval counter is done, bit 1 of the status word is set.

TABLE 40. µP/TEST INPUT BUS REGISTER (GWA = F807h)

P(15:0)	FUNCTION
15:0	This 16-bit value can be used as the input to one or more NCO/Mixer/CIC sections for test or to set the input to a constant value to minimize power when the channel is not in use. The $\overline{ENI}$ signal for this input is either bit 11 in the channel register at IWA *000h or the strobe generated by a write to location GWA F808h (selected via bit 12 of the channel register at IWA *000h).

TABLE 41. µP/TEST INPUT BUS $\overline{ENI}$ REGISTER (GWA = F808h)

P(15:0)	FUNCTION
N/A	A write to this location, generates and $\overline{ENI}$ strobe for the µP driven input port (when selected via bit 12 of IWA *000h).

TABLE 42. SYNCO STROBE REGISTER (GWA = F809h)

P(15:0)	FUNCTION
N/A	A write to this location will cause a one-clock-wide pulse on the SYNCO pin. The SYNCO pin is used to synchronize multiple channels or parts. The SYNCO pin from one part is typically connected to the SYNCI pin of all the parts. Up to two pipeline registers may be inserted in the SYNCO to SYNCI path.

TABLE 43. µP FIFO READ ORDER CONTROL REGISTER (GWA = F820h thru F83Fh)

P(15:0)	FUNCTION		
4:0	The five bits selecting the data type are encoded as follows: C C D D D, where CC is the channel number and DDD is the data type.		
	DDD	Data Type	
	000	I(23:8)	The upper 16 bits of the I data path via the FIFO/AGC.
	001	I(7:0),8*zeros	The lower 8 bits of the I data path.
	010	Q(23:8)	The upper 16 bits of the Q data path via the FIFO/AGC.
	011	Q(7:0),8*zero	The lower 8 bits of the Q data path.
	100	Mag(23:8)	The upper 16 bits of magnitude (after the gain adjust described in channel register)
	101	Mag(7:0),8*zero	The lower 8 bits of magnitude.
	110	Phase(15:0)	The upper 16 bits of phase.
	111	AGC gain (15:0)	The upper 16 bits of the AGC gain.

Table of Indirect Read Address (IRA) Registers

The address decoding for the read source locations is given below. The internal address of the data to be read is written to direct address 3 (ADD(2:0) = 3) to select and/or fetch the data. A strobe is generated, if needed, to fetch or stabilize the data for reading. If a strobe is needed, the indirect read address must be written to direct address 3 each time the data is needed. If a strobe is not needed, the data can be read repeatedly at direct addresses 0 and 1(ADD(2:0) = 0 and 1, respectively) with any changes in the data showing up immediately. The strobe to sample the AGC gain is generated separately by an indirect write (see IWA *00Fh in the Tables of Indirect Write Address Registers). This allows the AGC gain of all the channels to be sampled simultaneously.

NOTE: These Indirect Read Addresses are repeated for each channel. In the addresses below, the ***** field is the channel select nibble. These bits of the Indirect Address select the target channel register for the data being read. Values of 0 through 3 and F are valid.

TABLE 44. TABLE OF INDIRECT READ ADDRESS (IRA) REGISTERS

IRA	FUNCTION
*006h	Active Carrier NCO Center Frequency
*00Ch	Wait Preload, Decr 1&2
*009h	Active Timing NCO Center Freq (Most Significant 32 bits)
*00Fh	AGC gain
*100h - *17Fh	Instruction RAMs
*180h - *1FCh	Instruction RAMs (pointer DRAM)
*400h - *43Fh	Coefficient ROM -HBF, const.
*440h - *47Fh	Coefficient RAM -1
*480h - *4FFh	Coefficient RAM -2
*500h - *5FFh	Coefficient ROM -Resampler
F806h	Input Level Detector Output

Absolute Maximum Ratings

Supply Voltage . . . . . +6V
Input, Output or I/O Voltage . . . . . GND -0.5V to V_{CC} +0.5V
ESD Classification . . . . . Class III

Operating Conditions

Voltage Range . . . . . +3.15V to +3.45V
Temperature Range
Industrial. . . . . -40^oC to 85^oC
Input Low Voltage . . . . . 0V to +0.8V
Input High Voltage . . . . . 2V to V_{CC}

Thermal Information

Thermal Resistance (Typical)	θ_{JA} ($^oC/W$)
196 Lead BGA Package (Note 5)	27
w/200 LFM Air Flow	24
w/400 LFM Air Flow	23

Maximum Junction Temperature . . . . . 150^oC
Maximum Storage Temperature Range . . . . . -65^oC to 150^oC
Maximum Lead Temperature (Soldering 10s) . . . . . 300^oC

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

5. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications

V_{CC} = 3.3V ± 0.15V, T_A = -40^oC to 85^oC, Industrial

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
Logical One Input Voltage	V_{IH}	V_{CC} = 3.45V	2.0	-	V
Logical Zero Input Voltage	V_{IL}	V_{CC} = 3.15V	-	0.8	V
Output High Voltage	V_{OH}	I_{OH} = -2mA, V_{CC} = 3.15V	2.6	-	V
Output Low Voltage	V_{OL}	I_{OL} = 2mA, V_{CC} = 3.15V	-	0.4	V
Input Leakage Current	I_I	V_{IN} = V_{CC} or GND, V_{CC} = 3.45V	-10	10	µA
Output Leakage Current	I_O	V_{IN} = V_{CC} or GND, V_{CC} = 3.45V	-10	10	µA
Standby Power Supply Current	I_{CCSB}	V_{CC} = 3.45V, Outputs Not Loaded, No CLK	-	500	µA
Operating Power Supply Current	I_{CCOP}	f = 70MHz, V_{IN} = V_{CC} or GND, V_{CC} = 3.45V, Outputs Not Loaded	-	850	mA (Note 6)
Input Capacitance	C_{IN}	Freq = 1MHz, V_{CC} open, all measurements are referenced to device ground	-	7	pF (Note 7)
Output Capacitance	C_{OUT}		-	7	pF (Note 7)

NOTES:

6. Power Supply current is proportional to frequency of operation and programmed configuration of the part. Typical rating for I_{CCOP} is 11mA/MHz.
7. Capacitance: T_A = 25^oC, controlled via design or process parameters and not directly tested. Characterized upon initial design and at major process or design changes.

AC Electrical Specifications

V_{CC} = 3.3V ± 0.15V, T_A = -40^oC to 85^oC Industrial

PARAMETER	SYMBOL	MIN	MAX	UNITS
INPUT AND CONTROL TIMING				
CLK Frequency	f_{CLK}	-	70	MHz
CLK High	t_{CH}	5	-	ns
CLK Low	t_{CL}	5	-	ns
Setup Time - Data Inputs, Input Enables, SYNCI to CLK High	t_{DS}	6	-	ns
Hold Time - Data Inputs, Input Enables, SYNCI to CLK High	t_{DH}	0	-	ns
CLK to Output Valid - SYNCO, $\overline{INTRPT}$	t_{PDC}	-	6.5	ns
$\overline{RESET}$ Pulse Width Low	t_{RW}	5	-	ns
$\overline{RESET}$ Setup Time to CLK High (Note 8)	t_{RS}	6	-	ns
Output Rise, Fall Time (Note 9)	t_{RF}	-	3	ns

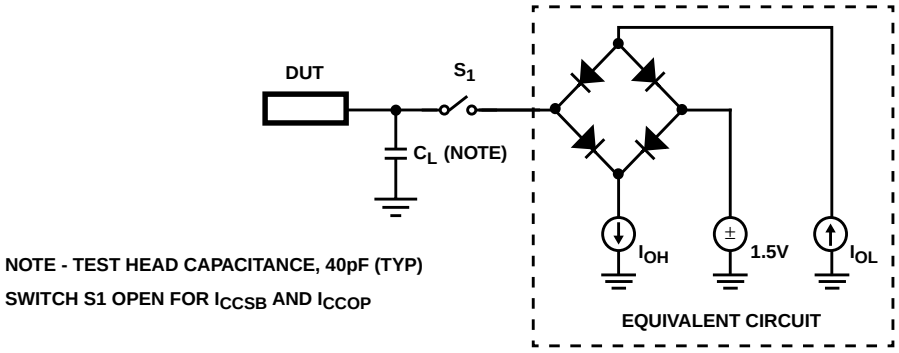
AC Electrical Specifications V_{CC} = 3.3V ± 0.15V, T_A = -40°C to 85°C Industrial **(Continued)**

PARAMETER	SYMBOL	MIN	MAX	UNITS
MICROPROCESSOR WRITE TIMING				
P(15:0) Setup Time to Rising Edge of $\overline{WR}$	t_{DSW}	10	-	ns
P(15:0) Hold Time from Rising Edge of $\overline{WR}$	t_{DHW}	-2	-	ns
A(1:0) Setup Time to Rising Edge of $\overline{WR}$	t_{ASW}	10	-	ns
A(1:0) Hold Time from Rising Edge of $\overline{WR}$	t_{AHW}	-2	-	ns
$\overline{CE}$ Setup Time to Rising Edge of $\overline{WR}$	t_{CSW}	10	-	ns
$\overline{CE}$ Hold Time from Rising Edge of $\overline{WR}$	t_{CHW}	-2	-	ns
$\overline{WR}$ Low Time	t_{WL}	5	-	ns
MICROPROCESSOR READ TIMING				
A(1:0) Setup Time to FALLING Edge of $\overline{RD}$	t_{ASR}	8	-	ns
A(1:0) Hold Time from RISING Edge of $\overline{RD}$	t_{AHR}	-2	-	ns
$\overline{RD}$ Enable Time	t_{RE}	-	11.5	ns
$\overline{RD}$ Disable Time (Note 9)	t_{RD}	-	8	ns
$\overline{RD}$ to P(15:0) Data Valid Time	t_{DV}	-	12	ns
$\overline{CE}$ Setup Time to Falling Edge of $\overline{RD}$	t_{CSR}	8	-	ns
$\overline{CE}$ Hold Time from Rising Edge of $\overline{RD}$	t_{CHR}	-2	-	ns
SERIAL CLOCK OUTPUT TIMING				
CLK to Serial Data, Sync and SCLK (Divide-by 2 thru 16 Modes)	t_{PD}	-	6.5	ns
CLK Low to SCLK Low (Divide-by 1 Mode, Note 9)	t_{PDL}	-	6.5	ns
CLK High to SCLK High (Divide-by 1 Mode, Note 9)	t_{PDH}	-	3	ns
Time Skew Between SCLK and Serial Data or Serial Sync (Divide-by 2 thru 16 Modes, Note 9)	t_{SKEW1}	-1	1	ns
Time Skew Between SCLK and Serial Data or Serial Sync (Divide-by 1 Mode, Note 9)	t_{SKEW2}	0.5	2	ns

NOTES:

8. The HSP50216 goes into reset immediately on $\overline{RESET}$ going low and comes out of reset on the 4th rising edge of CLK after $\overline{RESET}$ goes high.
9. Controlled via design or process parameters and not directly tested. Characterized upon initial design and at major process or design changes.

AC Test Load Circuit



NOTE - TEST HEAD CAPACITANCE, 40pF (TYP)

SWITCH S1 OPEN FOR I_{CCSB} AND I_{CCOP}

Waveforms

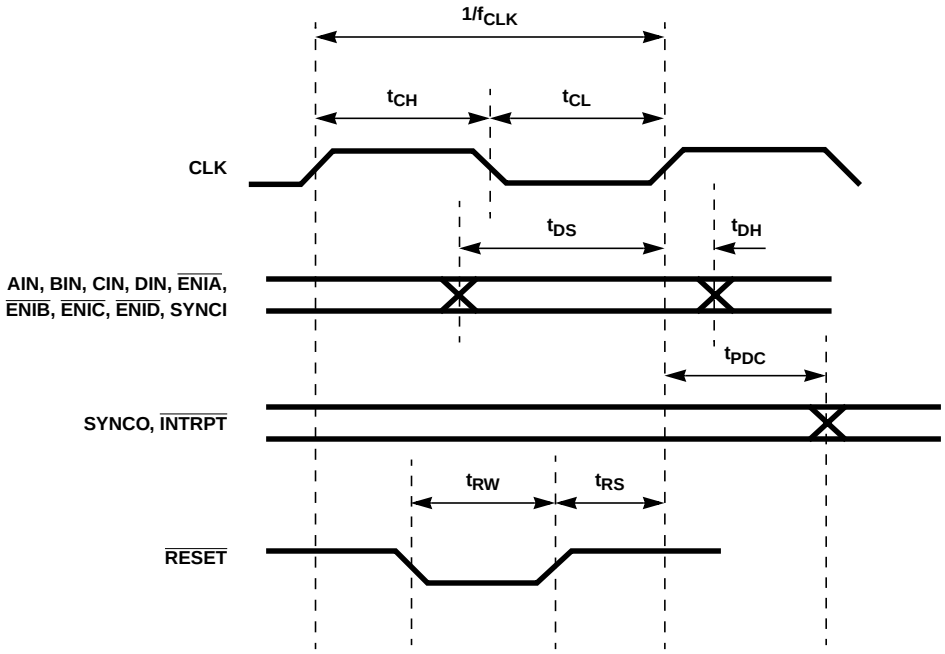


FIGURE 2. INPUT AND CONTROL TIMING

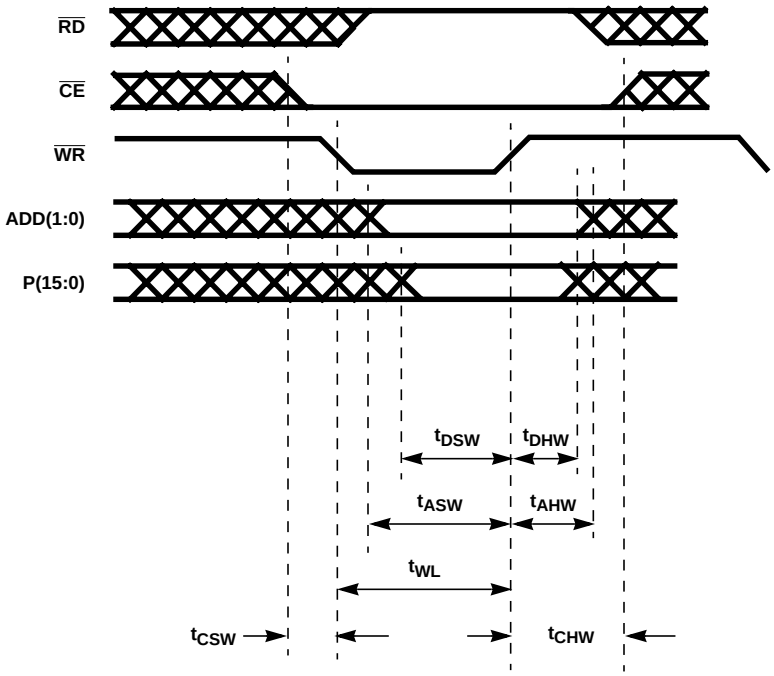


FIGURE 3. MICROPROCESSOR WRITE TIMING

Waveforms (Continued)

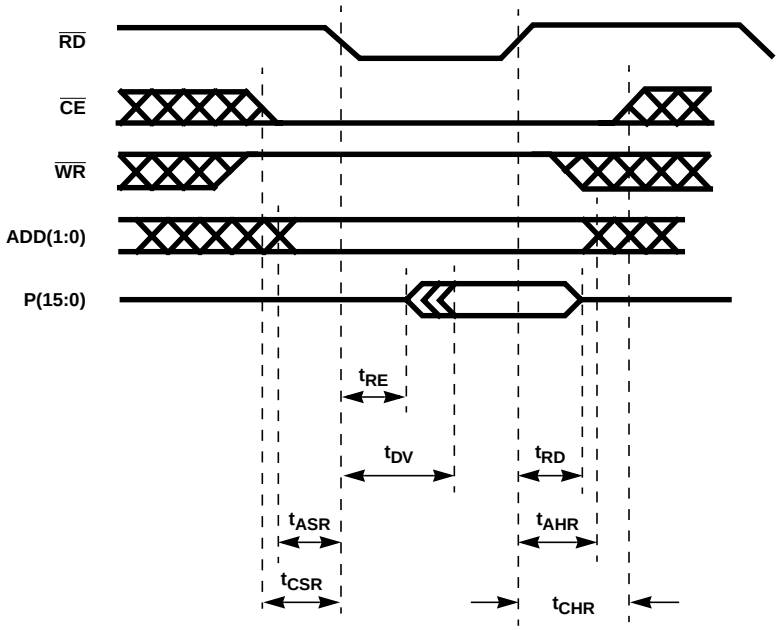


FIGURE 4. MICROPROCESSOR READ TIMING

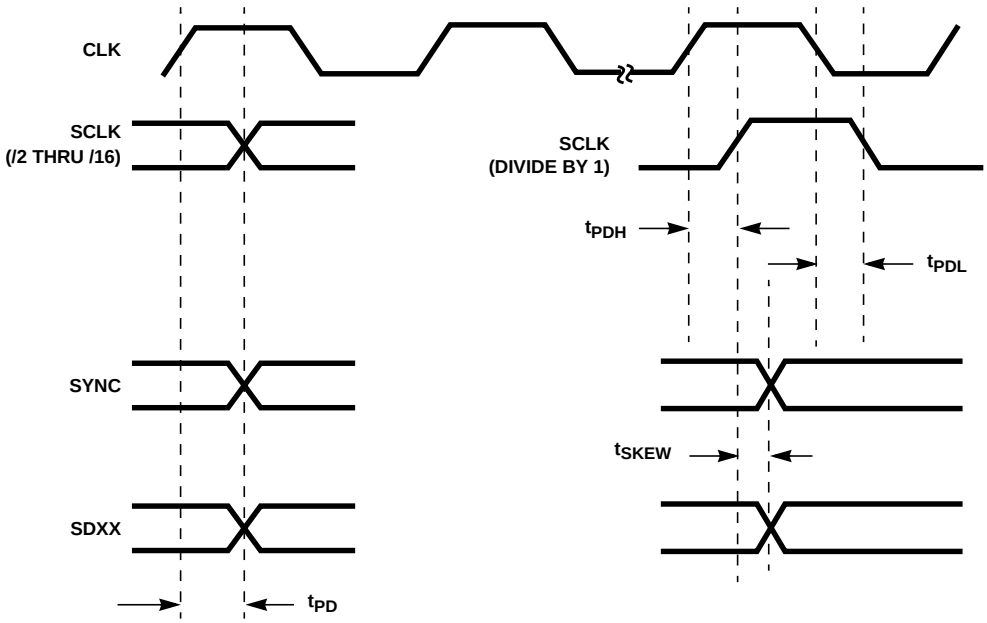


FIGURE 5. SERIAL OUTPUT TIMING

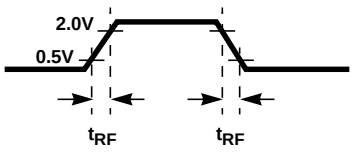


FIGURE 6. OUTPUT RISE AND FALL TIMES

ROMd FIR Filters - Response Curves

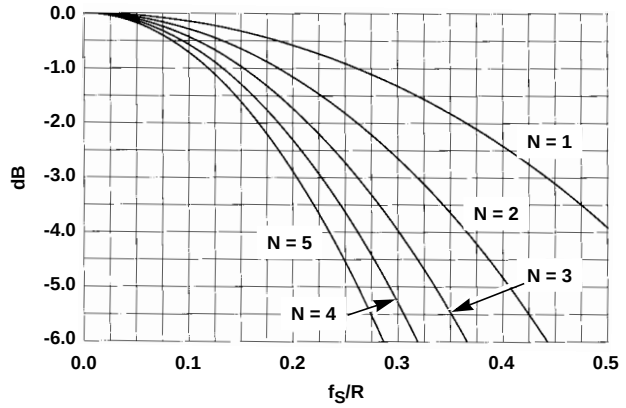


FIGURE 7. CIC PASSBAND ROLLOFF

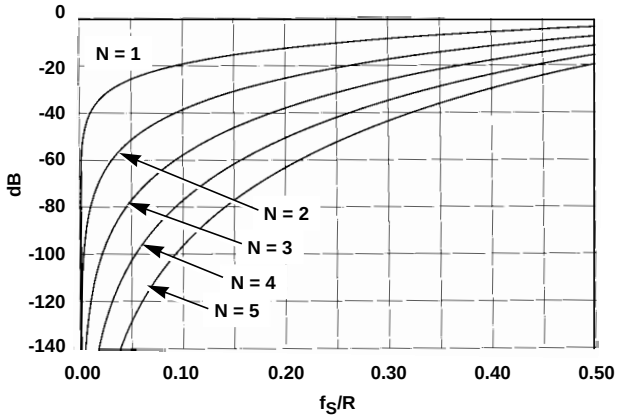


FIGURE 8. CIC FIRST ALIAS LEVEL

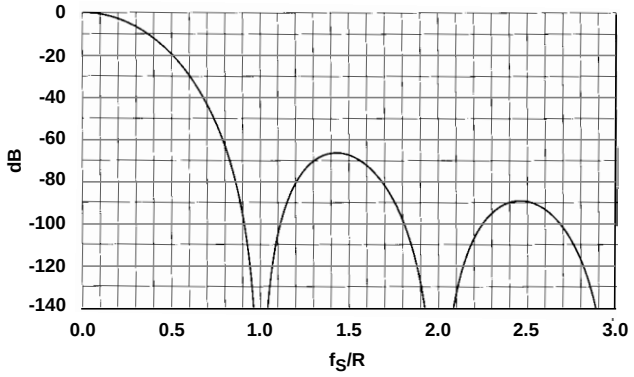
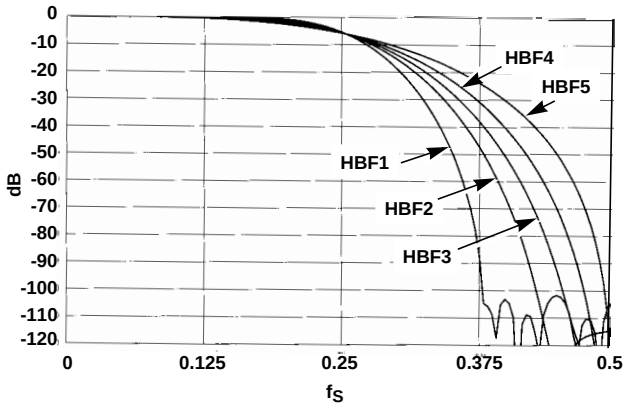
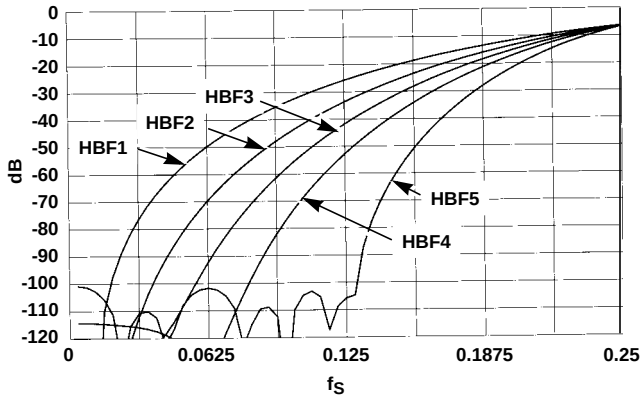


FIGURE 9. 5TH ORDER (N = 5) CIC RESPONSE



NOTE: HBF4 not included in the ROMd Fir Filter Coefficient memory. See Note 10 of Table 46.

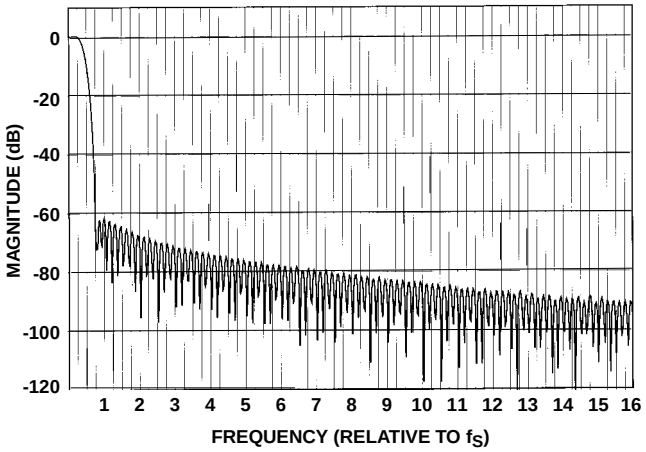
FIGURE 10. ROMd HALFBAND FILTER FREQUENCY RESPONSE



NOTE: HBF4 not included in the ROMd Fir Filter Coefficient memory. See Note 10 of Table 46.

FIGURE 11. ROMd HALFBAND FILTER ALIAS FREQUENCY RESPONSE

ROMd FIR Filters - Response Curves (Continued)



NOTE: There is a 65dB limitation in SNR using the Re-Sampler Filter.

FIGURE 12. POLYPHASE RESAMPLER FILTER BROADBAND FREQUENCY RESPONSE

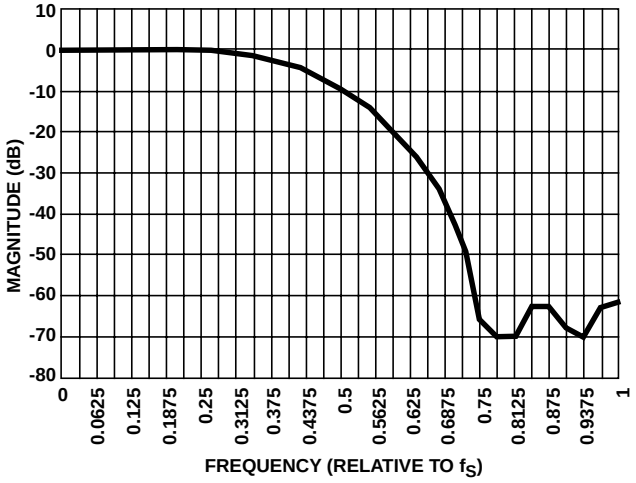


FIGURE 13. POLYPHASE RESAMPLER FILTER PASS BAND FREQUENCY RESPONSE

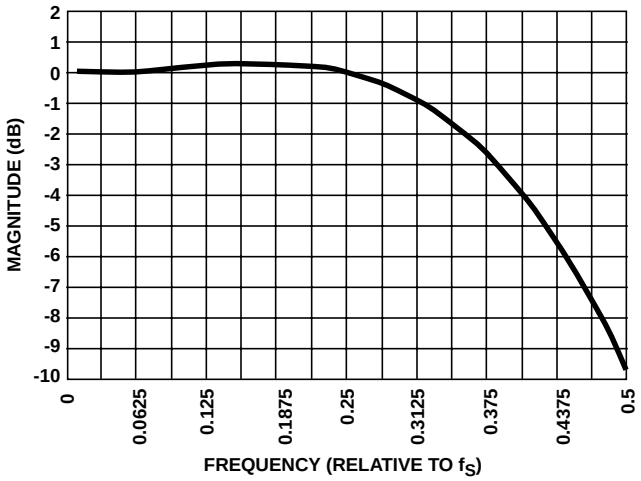


FIGURE 14. POLYPHASE RESAMPLER FILTER EXPANDED RESOLUTION PASSBAND FREQUENCY RESPONSE

TABLE 45. CIC PASSBAND AND ALIAS LEVELS

FREQUENCY	5TH ORDER		4TH ORDER		3RD ORDER		2ND ORDER		1ST ORDER	
f_S / R	PASSBAND	ALIAS	PASSBAND	ALIAS	PASSBAND	ALIAS	PASSBAND	ALIAS	PASSBAND	ALIAS
0	0	<-200	0	<-200	0	<-200	0	<-200	0	<-200
0.01	-0.007	-199.564	-0.006	-159.651	-0.004	-119.738	-0.003	-79.825	-0.001	-39.913
0.02	-0.029	-169.041	-0.023	-135.233	-0.017	-101.425	-0.011	-67.617	-0.006	-33.808
0.03	-0.064	-151.023	-0.051	-120.818	-0.039	-90.614	-0.026	-60.409	-0.013	-30.205
0.04	-0.114	-138.129	-0.091	-110.503	-0.069	-82.877	-0.046	-55.252	-0.023	-27.626
0.05	-0.179	-128.048	-0.143	-102.438	-0.107	-76.829	-0.071	-51.219	-0.036	-25.610
0.06	-0.257	-119.749	-0.206	-95.799	-0.154	-71.849	-0.103	-47.900	-0.051	-23.950
0.07	-0.351	-112.683	-0.280	-90.146	-0.210	-67.610	-0.140	-45.073	-0.070	-22.537
0.08	-0.458	-106.522	-0.367	-85.218	-0.275	-63.913	-0.183	-42.609	-0.092	-21.304
0.09	-0.580	-101.054	-0.464	-80.843	-0.348	-60.633	-0.232	-40.422	-0.116	-20.211
0.10	-0.717	-96.135	-0.573	-76.908	-0.430	-57.681	-0.287	-38.454	-0.143	-19.227
0.11	-0.868	-91.662	-0.694	-73.330	-0.521	-54.997	-0.347	-36.665	-0.174	-18.332
0.12	-1.034	-87.558	-0.827	-70.047	-0.620	-52.535	-0.413	-35.023	-0.207	-17.512
0.13	-1.214	-83.766	-0.971	-67.013	-0.728	-50.260	-0.486	-33.507	-0.243	-16.753
0.14	-1.409	-80.241	-1.127	-64.193	-0.846	-48.145	-0.564	-32.096	-0.282	-16.048
0.15	-1.619	-76.947	-1.295	-61.558	-0.972	-46.168	-0.648	-30.779	-0.324	-15.389
0.16	-1.844	-73.855	-1.475	-59.084	-1.107	-44.313	-0.738	-29.542	-0.369	-14.771
0.17	-2.084	-70.943	-1.667	-56.754	-1.251	-42.566	-0.834	-28.377	-0.417	-14.189
0.18	-2.340	-68.189	-1.872	-54.551	-1.404	-40.913	-0.936	-27.276	-0.468	-13.638
0.19	-2.610	-65.579	-2.088	-52.463	-1.566	-39.347	-1.044	-26.231	-0.522	-13.116
0.20	-2.896	-63.098	-2.317	-50.478	-1.737	-37.859	-1.158	-25.239	-0.579	-12.620
0.21	-3.197	-60.734	-2.558	-48.587	-1.918	-36.440	-1.279	-24.294	-0.639	-12.147
0.22	-3.514	-58.477	-2.811	-46.782	-2.108	-35.086	-1.406	-23.391	-0.703	-11.695
0.23	-3.847	-56.319	-3.077	-45.055	-2.308	-33.792	-1.539	-22.528	-0.769	-11.264
0.24	-4.195	-54.252	-3.356	-43.402	-2.517	-32.551	-1.678	-21.701	-0.839	-10.850
0.25	-4.560	-52.269	-3.648	-41.815	-2.736	-31.361	-1.824	-20.907	-0.912	-10.454
0.26	-4.941	-50.363	-3.953	-40.291	-2.965	-30.218	-1.976	-20.145	-0.988	-10.073
0.27	-5.338	-48.531	-4.271	-38.825	-3.203	-29.119	-2.135	-19.412	-1.068	-9.706
0.28	-5.752	-46.767	-4.602	-37.413	-3.451	-28.060	-2.301	-18.707	-1.150	-9.353
0.29	-6.183	-45.066	-4.946	-36.053	-3.710	-27.040	-2.473	-18.026	-1.237	-9.013
0.30	-6.631	-43.426	-5.305	-34.740	-3.978	-26.055	-2.652	-17.370	-1.326	-8.685
0.31	-7.096	-41.842	-5.677	-33.473	-4.257	-25.105	-2.838	-16.737	-1.419	-8.368
0.32	-7.578	-40.311	-6.063	-32.249	-4.547	-24.187	-3.031	-16.125	-1.516	-8.062
0.33	-8.078	-38.832	-6.463	-31.066	-4.847	-23.299	-3.231	-15.533	-1.616	-7.766
0.34	-8.596	-37.401	-6.877	-29.921	-5.158	-22.440	-3.439	-14.960	-1.719	-7.480
0.35	-9.133	-36.015	-7.306	-28.812	-5.480	-21.609	-3.653	-14.406	-1.827	-7.203
0.36	-9.688	-34.674	-7.750	-27.739	-5.813	-20.804	-3.875	-13.869	-1.938	-6.935
0.37	-10.262	-33.374	-8.209	-26.699	-6.157	-20.024	-4.105	-13.349	-2.052	-6.675
0.38	-10.854	-32.114	-8.684	-25.691	-6.513	-19.268	-4.342	-12.845	-2.171	-6.423
0.39	-11.467	-30.892	-9.174	-24.713	-6.880	-18.535	-4.587	-12.357	-2.293	-6.178
0.40	-12.099	-29.707	-9.679	-23.766	-7.260	-17.824	-4.840	-11.883	-2.420	-5.941
0.41	-12.752	-28.557	-10.201	-22.846	-7.651	-17.134	-5.101	-11.423	-2.550	-5.711
0.42	-13.425	-27.442	-10.740	-21.953	-8.055	-16.465	-5.370	-10.977	-2.685	-5.488
0.43	-14.119	-26.359	-11.295	-21.087	-8.472	-15.815	-5.648	-10.544	-2.824	-5.272
0.44	-14.835	-25.308	-11.868	-20.246	-8.901	-15.185	-5.934	-10.123	-2.967	-5.062
0.45	-15.573	-24.287	-12.458	-19.430	-9.344	-14.572	-6.229	-9.715	-3.115	-4.857
0.46	-16.333	-23.296	-13.066	-18.637	-9.800	-13.978	-6.533	-9.318	-3.267	-4.659
0.47	-17.116	-22.334	-13.693	-17.867	-10.270	-13.400	-6.847	-8.933	-3.423	-4.467
0.48	-17.923	-21.399	-14.339	-17.119	-10.754	-12.840	-7.169	-8.560	-3.585	-4.280
0.49	-18.754	-20.492	-15.003	-16.393	-11.253	-12.295	-7.502	-8.197	-3.751	-4.098
0.50	-19.610	-19.610	-15.688	-15.688	-11.766	-11.766	-7.844	-7.844	-3.922	-3.922

TABLE 46. DECIMATING HALFBAND FIR FILTER COEFFICIENTS

	DECIMATING HALFBAND #1 (DHBF #1, 7-TAP)		DECIMATING HALFBAND #2 (DHBF #2, 11-TAP)		DECIMATING HALFBAND #3 (DHBF #3, 15-TAP)		DECIMATING HALFBAND #4 (DHBF #4, 19-TAP)		DECIMATING HALFBAND #5 (DHBF #1, 23-TAP)	
COEFF	HEX	DECIMAL	HEX	DECIMAL	HEX	DECIMAL	HEX	DECIMAL	HEX	DECIMAL
C0	FBFE40	- 0.031303406	00C250	0.005929947	FFD538	-0.00130558	000C68	0.000378609	FFF4A0	-0.000347137
C1	000000	0.000000000	000000	0.000000000	000000	0.000000000	000000	0.000000000	000000	0.000000000
C2	240100	0.281280518	F9B930	-0.049036026	0195A8	0.012379646	FF8320	-0.003810883	00525A	0.00251317
C3	3FFE80	0.499954224	000000	0.000000000	000000	0.000000000	000000	0.000000000	000000	0.000000000
C4	240100	0.281280518	258400	0.29309082	F83FE0	-0.06055069	0276A0	0.019245148	FEB320	-0.010158539
C5	000000	0.000000000	3FFF00	0.499969482	000000	0.000000000	000000	0.000000000	000000	0.000000000
C6	FBFE40	- 0.031303406	258400	0.29309082	265480	0.299453735	F70D60	-0.069904327	03E920	0.03055191
C7			000000	0.000000000	3FFE80	0.499954224	000000	0.000000000	000000	0.000000000
C8			F9B930	-0.049036026	265480	0.299453735	26EC80	0.304092407	F581A0	-0.081981659
C9			000000	0.000000000	000000	0.000000000	400000	0.500000000	000000	0.000000000
C10			00C250	0.005929947	F83FE0	-0.06055069	26EC80	0.304092407	279B00	0.309417725
C11					000000	0.000000000	000000	0.000000000	400000	0.500000000
C12					0195A8	0.012379646	F70D60	-0.069904327	279B00	0.309417725
C13					000000	0.000000000	000000	0.000000000	000000	0.000000000
C14					FFD538	-0.00130558	0276A0	0.019245148	F581A0	-0.081981659
C15							000000	0.000000000	000000	0.000000000
C16							FF8320	-0.003810883	03E920	0.03055191
C17							000000	0.000000000	000000	0.000000000
C18							000C68	0.000378609	FEB320	-0.010158539
C19									000000	0.000000000
C20									00525A	0.00251317
C21									000000	0.000000000
C22									FFF4A0	-0.000347137

NOTES:

10. Decimating Halfband Filter #4 Coefficients are shown for reference only and if it is desired to implement this FIR filter these coefficients would have to be loaded into the FIR Coefficient RAM (They are not included in the ROMd Fir Filter Coefficient memory).

11. The 22-bit ROMd FIR filter coefficients are located in the upper 22 bits of the Read register when read back from ROM memory (except for Halfband #4). These bits occupy the upper six bytes (24 bits) with the two LSBs of the lower byte (bits 9:8 of 31:0) being zero. The decimal value for the hexadecimal coefficient is calculated by first converting the hexadecimal value to decimal and the dividing by 2^{23} (8388608).

TABLE 47. INTERPOLATING HALFBAND FIR FILTER COEFFICIENTS

	INTERPOLATING HALFBAND #2 (IHBF #2, 15-TAP)		INTERPOLATING HALFBAND #1 (IHBF #1, 23-TAP)	
COEFF	HEX	DECIMAL	HEX	DECIMAL
C0	FFAA24	-0.002620220	FFE944	-0.000693798
C1	000000	0.000000000	000000	0.000000000
C2	032B60	0.024761200	00A4B4	0.005026340
C3	000000	0.000000000	000000	0.000000000
C4	F07F40	-0.121116638	FD6640	-0.020317078
C5	000000	0.000000000	000000	0.000000000
C6	4CAB00	0.598968506	07D240	0.061103821
C7	800000	1.000000000	000000	0.000000000
C8	4CAB00	0.598968506	EB0340	-0.163963318
C9	000000	0.000000000	000000	0.000000000
C10	F07F40	-0.121116638	4F3600	0.618835449
C11	000000	0.000000000	800000	1.000000000
C12	032B60	0.024761200	4F3600	0.618835449
C13	000000	0.000000000	000000	0.000000000
C14	FFAA24	-0.002620220	EB0340	-0.163963318
C15			000000	0.000000000
C16			07D240	0.061103821
C17			000000	0.000000000
C18			FD6640	-0.020317078
C19			000000	0.000000000
C20			00A4B4	0.005026340
C21			000000	0.000000000
C22			FFE944	-0.000693798

NOTE:

12. The 22-bit ROMd FIR filter coefficients are located in the upper 22 bits of the Read register when read back from ROM memory. These bits occupy the upper six bytes (24 bits) with the two LSBs of the lower byte (bits 9:8 of 31:0) being zero. The decimal value for the hexadecimal coefficient is calculated by first converting the hexadecimal value to decimal and the dividing by 2^{23} (8388608).

TABLE 48. RESAMPLER FIR FILTER COEFFICIENTS

COEFF	HEX	DECIMAL	COEFF	HEX	DECIMAL	COEFF	HEX	DECIMAL
C 0 / 191	004000	0.001953125	C 32 / 159	FA3540	-0.045249939	C 64 / 127	0C2400	0.094848633
C 1 / 190	006910	0.003206253	C 33 / 158	F97F00	-0.050811768	C 65 / 126	0F8600	0.121276855
C 2 / 189	007A90	0.003740311	C 34 / 157	F8C4C0	-0.056495667	C 66 / 125	131700	0.149139404
C 3 / 188	008C90	0.004289627	C 35 / 156	F80880	-0.062240601	C 67 / 124	16D400	0.178344727
C 4 / 187	009ED0	0.004846573	C 36 / 155	F74C40	-0.067985535	C 68 / 123	1ABA00	0.208801270
C 5 / 186	00B0E0	0.005397797	C 37 / 154	F691C0	-0.073677063	C 69 / 122	1EC500	0.240386963
C 6 / 185	00C230	0.005926132	C 38 / 153	F5DB80	-0.079238892	C 70 / 121	22F100	0.272979736
C 7 / 184	00D240	0.006416321	C 39 / 152	F52C00	-0.084594727	C 71 / 120	273A00	0.306457520
C 8 / 183	00E090	0.006853104	C 40 / 151	F48600	-0.089660645	C 72 / 119	2B9900	0.340606689
C 9 / 182	00ECC0	0.007225037	C 41 / 150	F3EC00	-0.094360352	C 73 / 118	300A00	0.375305176
C 10 / 181	00F620	0.007511139	C 42 / 149	F36140	-0.098594666	C 74 / 117	348800	0.410400391
C 11 / 180	00FBC0	0.007682800	C 43 / 148	F2E880	-0.102279663	C 75 / 116	390C00	0.445678711
C 12 / 179	00FCB0	0.007711411	C 44 / 147	F284C0	-0.105323792	C 76 / 115	3D9100	0.480987549
C 13 / 178	00F970	0.007612228	C 45 / 146	F23980	-0.107620239	C 77 / 114	420F00	0.516082764
C 14 / 177	00EFF0	0.007322311	C 46 / 145	F20940	-0.109092712	C 78 / 113	468200	0.550842285
C 15 / 176	00E050	0.006845474	C 47 / 144	F1F7C0	-0.109626770	C 79 / 112	4AE200	0.585021973
C 16 / 175	00C980	0.006149292	C 48 / 143	F20800	-0.109130859	C 80 / 111	4F2A00	0.618469238
C 17 / 174	00AAD0	0.005212784	C 49 / 142	F23C80	-0.107528687	C 81 / 110	535200	0.650939941
C 18 / 173	0083B0	0.004018784	C 50 / 141	F298C0	-0.104713440	C 82 / 109	575400	0.682250977
C 19 / 172	005370	0.002546310	C 51 / 140	F31F00	-0.100616455	C 83 / 108	5B2B00	0.712249756
C 20 / 171	0019A0	0.000782013	C 52 / 139	F3D280	-0.095138550	C 84 / 107	5ED000	0.740722656
C 21 / 170	FFD590	-0.001295090	C 53 / 138	F4B500	-0.088226318	C 85 / 106	623E00	0.767517090
C 22 / 169	FF86F0	-0.003694534	C 54 / 137	F5C900	-0.079803467	C 86 / 105	656E00	0.792419434
C 23 / 168	FF2D90	-0.006422043	C 55 / 136	F71040	-0.069816589	C 87 / 104	685D00	0.815338135
C 24 / 167	FEC930	-0.009485245	C 56 / 135	F88C40	-0.058219910	C 88 / 103	6B0500	0.836090088
C 25 / 166	FE59C0	-0.012886047	C 57 / 134	FA3E80	-0.044967651	C 89 / 102	6D6200	0.854553223
C 26 / 165	FDDF80	-0.016616821	C 58 / 133	FC27C0	-0.030036926	C 90 / 101	6F7000	0.870605469
C 27 / 164	FD5A60	-0.020679474	C 59 / 132	FE48C0	-0.013404846	C 91 / 100	712C00	0.884155273
C 28 / 163	FCCB00	-0.025054932	C 60 / 131	00A140	0.004920959	C 92 / 99	729200	0.895080566
C 29 / 162	FC31F0	-0.029726028	C 61 / 130	033140	0.024940491	C 93 / 98	73A100	0.903350830
C 30 / 161	FB9000	-0.034667969	C 62 / 129	05F7C0	0.046623230	C 94 / 97	745600	0.908874512
C 31 / 160	FAE600	-0.039855957	C 63 / 128	08F400	0.069946289	C 95 / 96	74B200	0.911682129

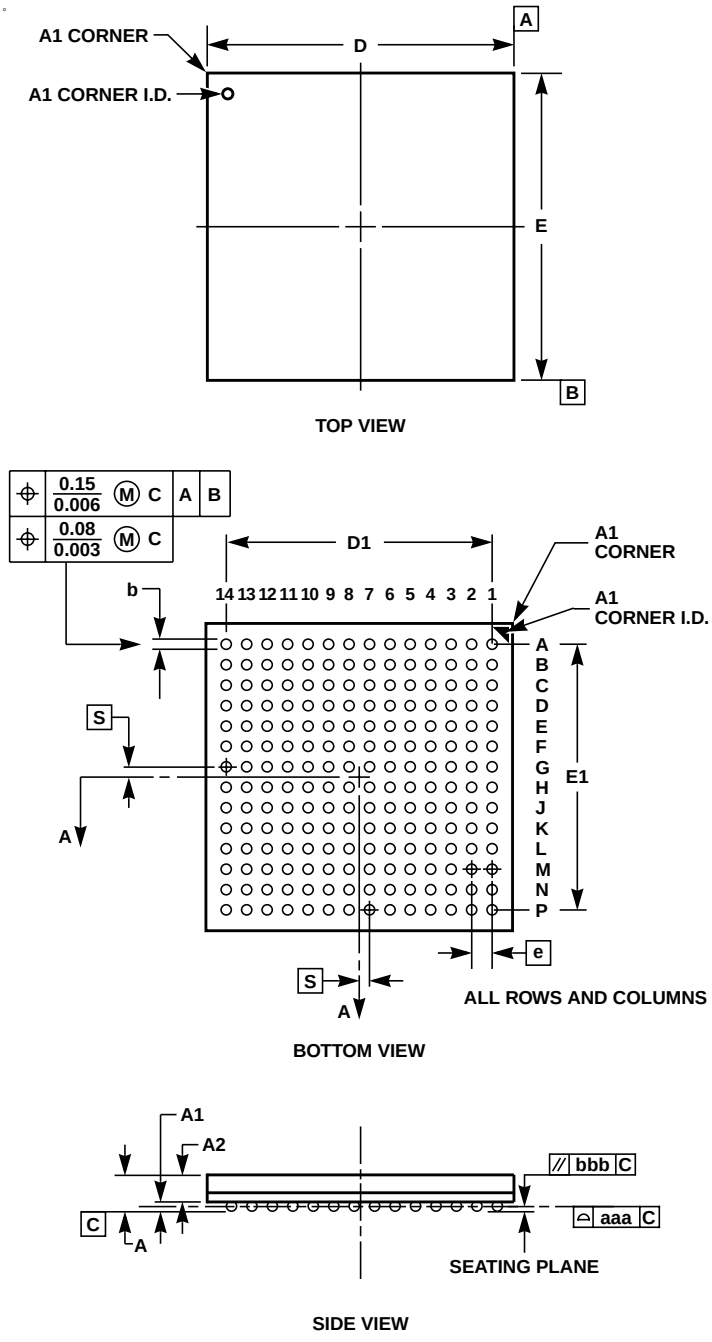
NOTE:

13. The 22-bit ROMd FIR filter coefficients are located in the upper 22 bits of the Read register when read back from ROM memory. These bits occupy the upper six bytes (24 bits) with the two LSBs of the lower byte (bits 9:8 of 31:0) being zero. The decimal value for the hexadecimal coefficient is calculated by first converting the hexadecimal value to decimal and the dividing by 2^{23} (8388608).

TABLE 49. BIT WEIGHTING FOR AGC LOOP FEEDBACK PATH

AGC ACCUM BIT POSITION	GAIN ERROR INPUT	GAIN ERROR BIT WEIGHT	AGC LOOP FILTER GAIN (MANTISSA)	AGC LOOP FILTER GAIN MULTIPLIER (OUTPUT)	AGC LOOP FILTER GAIN (EXPONENT)				AGC BIT WEIGHTS			AGC GAIN RESOLUTION (dB)
					SHIFT = 0	SHIFT = 4	SHIFT = 8	SHIFT = 15	LIMITS	TO OUTPUT SECTION	TO µP	
31					2	2	2	2		0	0	
30					2	2	2	2	3	E	E	48
29					2	2	2	2	2	E	E	24
28					2	2	2	2	1	E	E	12
27	15	= 2		2	2	2	2	2	0	E	E	6
26	14	= 1		1	2	2	2	1	-1	M	M	3
25	13	= 0.	0.	0.	2	2	2	0.	-2	M	M	1.5
24	12	= 1	x	1	2	2	2	1	-3	M	M	0.75
23	11	= 2	x	2	2	2	2	2	-4	M	M	0.375
22	10	= 3	x	3	2	2	2	3	-5	M	M	0.1875
21	9	= 4	x	4	2	2	2	4	-6	M	M	0.09375
20	8	= 5		5	2	2	2	5	-7	M	M	0.04688
19	7	= 6		6	2	2	1	6	-8	M	M	0.02344
18	6	= 7		7	2	2	0.	7	-9	M	M	0.01172
17	5	= 8		8	2	2	1	8	-10	M	M	0.00586
16	4	= 9		9	2	2	2	9	-11	M	M	0.00293
15	3	= 10		10	2	1	3	10	-12	M		0.00146
14	2	= 11		11	2	0.	4	11		M		0.000732
13	1	= 12		12	2	1	5	12		M		0.000366
12	0	= 13		13	2	2	6	13				0.000183
11				14	1	3	7	14				0.0000916
10					0.	4	8	G				0.0000458
9					1	5	9	G				0.0000229
8					2	6	10	G				0.0000114
7					3	7	11	G				0.00000572
6					4	8	12	G				0.00000286
5					5	9	13	G				
4					6	10	14	G				
3					7	11	G	G				
2					8	12	G	G				
1					9	13	G	G				
0					10	14	G	G				

Plastic Ball Grid Array Packages (BGA)



V196.12x12

196 BALL PLASTIC BALL GRID ARRAY PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.059	-	1.50	-
A1	0.012	0.016	0.31	0.41	-
A2	0.038	0.044	0.96	1.11	-
b	0.016	0.020	0.41	0.51	7
D/E	0.468	0.476	11.90	12.10	-
D1/E1	0.405	0.413	10.30	10.50	-
N	196		196		-
e	0.032 BSC		0.80 BSC		-
MD/ME	14 x 14		14 x 14		3
bbb	0.004		0.10		-
aaa	0.005		0.12		-

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NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. “MD” and “ME” are the maximum ball matrix size for the “D” and “E” dimensions, respectively.
4. “N” is the maximum number of balls for the specific array size.
5. Primary datum C and seating plane are defined by the spherical crowns of the contact balls.
6. Dimension “A” includes standoff height “A1”, package body thickness and lid or cap height “A2”.
7. Dimension “b” is measured at the maximum ball diameter, parallel to the primary datum C.
8. Pin “A1” is marked on the top and bottom sides adjacent to A1.
9. “S” is measured with respect to datum’s A and B and defines the position of the solder balls nearest to package centerlines. When there is an even number of balls in the outer row the value is “S” = e/2.

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